Design For Manufacturing

CONTENTS

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Section A: INTRODUCTION

This manual provides an overview of the requirements for the Design for Manufacturability (DFM) and reliability for rigid multilayer boards.

Manufacturability is the practice of designing circuit board products that meet not only the capabilities of the customer's assembly manufacturing process but also the capabilities of the board fabrication process. Some of the benefits of designing for manufacturability are:

- Higher quality
- Reduced lead times
- Lower labor and material costs
- Higher first pass yields
- Minimized environmental impact

To achieve these benefits, this manual has been developed to enable a circuit board designer to understand the key cost drivers relative to bare board manufacture. The cost drivers are:

- Raw laminate - both panel utilization and material selection
- Complexity factors (component/design technology)
- Total number of holes
- Gold requirements
- Solder mask requirements
- Electrical test parameters
- Yield
- Minimized environmental impact

Section B: RAW MATERIALS SELECTION

Material Selection and Panel Utilization

Objective

This section communicates guidelines for selecting materials for multilayer boards which not only meet customer performance characteristics but also minimize manufacturability issues such as bow and twist and misregistration.

Raw laminate is the single largest cost component in a multilayer board. Optimizing its construction around standard base materials and achieving maximum material utilization based on the usable area available on standard panel sizes can have a significant positive impact on multilayer board prices and deliveries.

When specifying dielectric thickness, as is required for impedance reasons for example, this dimension should be selected from base laminates or prepreg thickness that is available from REYcomp. Page B-3 of this manual lists multilayer materials ranging in thickness from .005" to .042". Certain low power applications and continuing circuit densification of multilayer boards, makes the availability of thin laminates of .004" or less necessary. These thin (also called ultrathin) laminates are only available with a single ply of glass fabric.

The requirement for alternative materials should not discourage the designer from generating requests. Often, alternative and cost effective options can be provided in conjunction with continuing development engineering efforts at REYcomp.

REYcomp Corporation is committed to Environmentally-Conscious Manufacturing (ECM) and encourages customers to utilize designs and processes that are less wasteful *whenever possible. As examples, the use of the lightest copper weight (0.5 ounce) results in the least use of chemicals and generation of waste by-products. The choice of soldermask affects the amount and toxicity of solvent used and emitted. The choice of Anti-tarnish instead of Hot Air Solder Leveling (HASL) reduces the use of lead and emission from flux and fusing oil. ECM processes are indicated in this manual by the symbol* ‡.

Material Properties

CORE CONSTRUCTION

- FR-4, E-glass reinforced*, bifunctional or tetrafunctional epoxy resin.
- Megtron , E-glass reinforced*, epoxy/polyphenylene oxide resin.

MATERIAL PROPERTIES	VALUES	
	FR-4	Megtron
ELECTRICAL		
Dielectric Constant @ 1 Mhz	4.3 - 4.9**	3.5 - 4.2**
Dissipation Factor @ 1 Mhz	.017-.021**	.010-.015**
Dielectric Strength V/mi	750	1100
Surface Resistance Ω	10^{12}	10^{10}
Volume Resistivity Ω cm	10^{13}	10^{12}
THERMAL		
Glass Transition Temp (°C)	140	180
Z-Axis Expansion % (1)	5.5	4.5
PHYSICAL		
CTE X/Y PPM	16/16	13/13
Moisture Absorption %	0.05 - 0.10	0 .80
Flammability - U.L.	VO	VO

* See following prepreg section for glass styles

** Values directly related to glass to resin ratio.

(1) This is the Z-axis expansion of the resin material from 25°C to 275°C. For ref., copper Z-axis expansion is 0.5%.

FR-4 Base Material and Thickness

Core	Copper Weight (oz)	Nominal Mtl. Thickness (in.)	Measured Mtl. Thickness (in.)
(Base Material with copper)		(Base Material)	
5	0.5/0.5	.005 +/- .001	.005
6	0.5/0.5	.006 +/- .001	.0056
8	0.5/0.5	.008 +/- .001	.0074
10	0.5/0.5	.010 +/- .0015	.009
12	0.5/0.5	.012 +/- .0015	.0113
15	0.5/0.5	.015 +/- .002	.0141
21	0.5/0.5	.025 +/- .0025	.0249
28	0.5/0.5	.028 +/- .0025	.0282
42	1/1	.042 +/- .005	.0421

The above is a listing of most commonly used FR-4 materials for multilayer boards. Thickness of GETEK® and Megtron materials are similar. Other core material and copper thicknesses are available. Contact REYcomp Application Engineer or Account Manager for specific data.

FR-4 Prepreg Designation and Thickness

Prepreg or "B-Stage" is the bonding material used during the construction of multilayer boards. REYcomp currently utilizes five types of prepreg with 106, 1080, 2116, 1500 and 7628 glass styles.

Prepreg properties (after full cure) are identical to those listed for base materials on page B-2.

Due to various limitations as to the number of plies and/or types of prepreg that can be utilized between layers of a board, specific applications need to be discussed with REYcomp Application Engineering.

Glass Style	Pressed Thickness
106	.0021
1080	.0031
2116	.0053
1500	.0062
7628	.0076

Thicknesses of GETEK® and Megtron prepregs are similar. Contact REYcomp Application Engineer or Account Manager for specific data.

Copper Clad for Materials

Type: Electrodeposited copper, drum side out, high-temperature-elongation.

The copper clad FR-4 material is conventionally specified by its ounce- weight per foot^2.

Nominal Thickness: 0.25 oz. = .0035" (8.75μm) ‡

0.5 oz. = .007" (17.5 μm)

1.0 oz = .0014" (35 μm)

2.0 oz = .0028" (70 μm)

If current carrying capacity permits, the specification of 0.5 ounce copper needs to be considered in all cases.* The advantages are:

- Reduced dimensional variation of etched features.
- Higher impedance for a given line width, less impedance variation.
- Thinner dielectric thickness for a given impedance, resulting in a thinner board.
- Reduction of copper waste generation and recycling effort by 50%. Reduced environmental impact‡.

* External layers will be electroplated with additional copper to a total thickness of .0014" (1 oz) minimum.

Resistivity of Copper

With designs of finer lines, distributed resistance of copper is becoming increasingly important. The formula for computing resistivity in copper traces is given by the following equation:

$$\mathbf{R = (0.679 \times 10^{-6}\ ohm/inch)\ /(width \times thickness\ inches \times Length)}$$

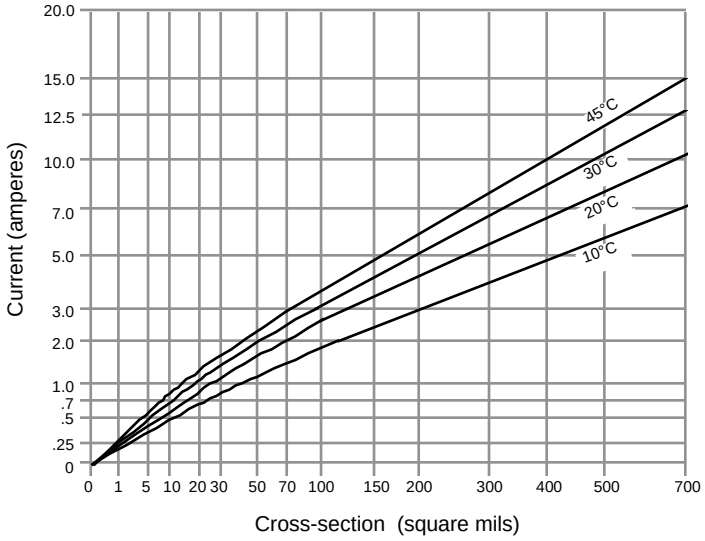
Example: In fine-line designs, using 0.5 oz. copper, a .005" trace, 5 inches long, the resistivity will be:

$$\mathbf{(.679 \times 10^{-6}) / ((5 \times 0.7 \times 10^{6})) \times 5 = 0.97\Omega}$$

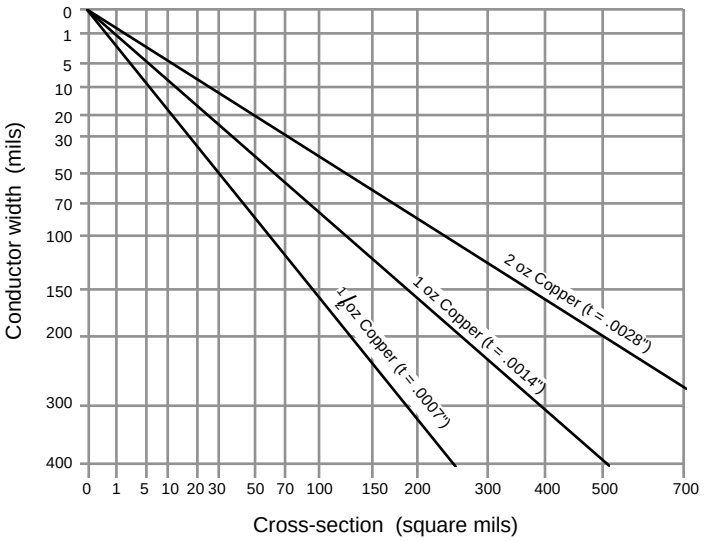
Current Carrying Capacity of Copper

The graphs are provided to reference the current carrying capacity for internal layers for common copper thickness and various temperature rises above ambient. Current carrying capacity of external layers is approximately 2X of that given for internal layers.

Encapsulated Conductor



Conductor Width (w) vs Cross-section



For detailed data on line widths and spacing requirements, see IPC-D-275 or MIL-STD-275.

Panel Sizes and Usable Area

There are three preferred panel sizes, 16 x 18 inches, 18 x 24 inches, and 21 x 24 inches. Larger panel size provides the most effective cost per unit area processed. Other panel sizes are available for special applications.

Note: Processing of GETEK ® material is currently limited to a panel size 18 x 24 inches.

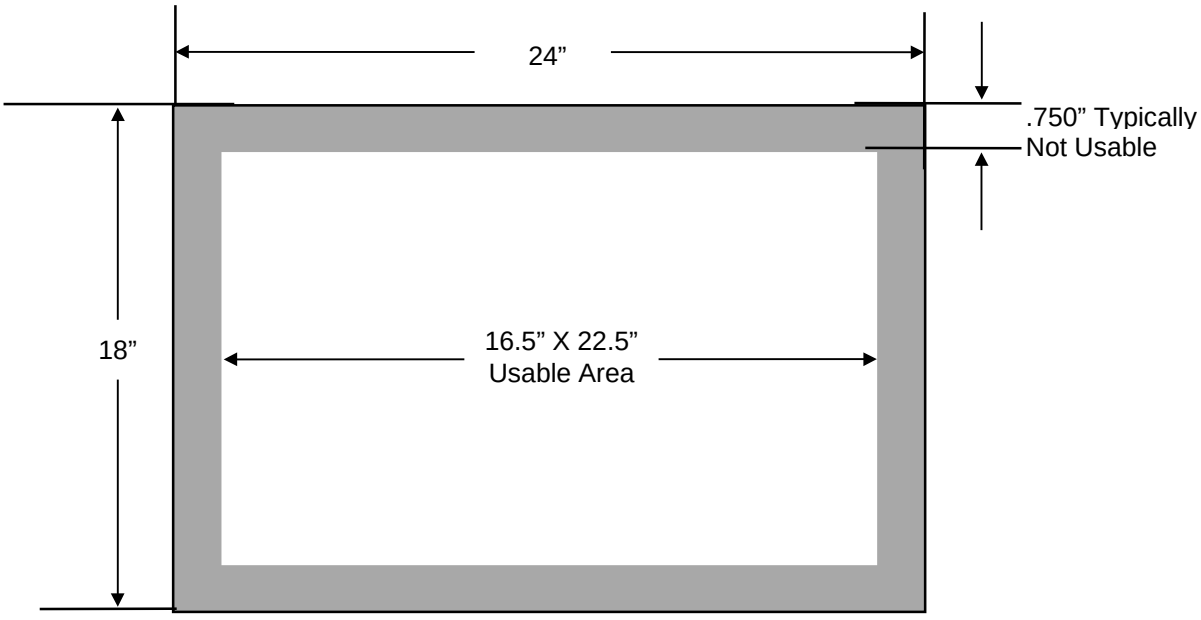
- The most effective material utilization will be achieved with boards or arrays of boards having their finished outline fit as efficiently as possible within the usable area of the panel‡ (see page B-9). Customer test coupons must be within the usable area.

- If the entire panel is shipped to the customer, the customer may negotiate to have locating holes and/or break-away tabs for insertion or surface mount equipment located outside the usable area. This is usually accomplished via the tab-routing process (see page C-22).

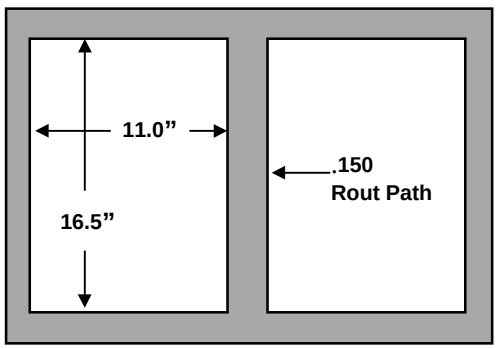
- Material utilization may be increased by utilizing the scoring process. This process places grooves on opposite sides of the panel between boards for the purpose of snapping the boards from the panel. Since boards can be “butted up” against each other, eliminating the real-estate for rout paths, more boards may be placed on the panel. This process also allows the entire panel to be shipped to the customer (see page C-23).

Multilayer Usable Area Diagrams

FOR MULTILAYER CIRCUIT BOARDS, A BORDER AREA OF .750 INCH AROUND THE CANNOT BE USED FOR ANY PART OF THE FINISHED CIRCUIT

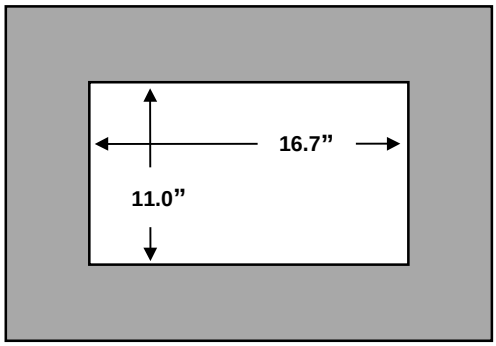


Example: Usable Area of 18” x 24”



Excellent Panel Utilization (84%)

Panel Price $160.00
Board Price $80.00



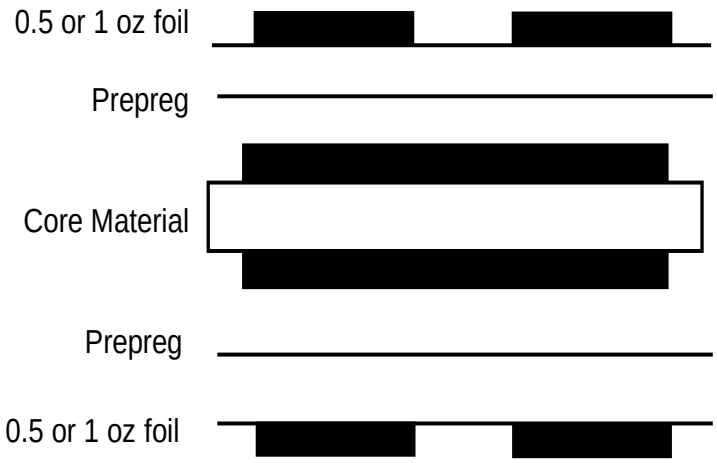
Poor Panel Utilization (33%)

Panel Price $160.00
Board Price $160.00

Example of 18” x 24” Panel Utilization

Multilayer Lay-up Recommendation

Unless the customer design dictates otherwise, Foil lamination is the method of choice assigned by REYcomp. It is the most cost effective manufacturing process and minimizes potential for bow and twist.



Example of Foil Lamination (4 Layer)

Multilayer Lay-up

1. Design multilayer boards with an even number of layers.

2. If specifying dielectric thickness, as may be required for impedance reasons for example, the dimensions should be selected from core or prepreg thicknesses that are available from REYcomp (see Pages B-3 & B-4).

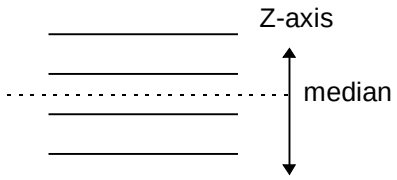
   Dielectric thicknesses made up of prepreg depend on the type or the combination of different types of these materials. REYcomp will advise you of what combination of prepreg is suitable and of achievable dimensions and tolerances.

   It is beneficial to discuss special dielectric requirements with REYcomp during the design stage if possible. This will allow time for material procurement if necessary. Also, manufacturing concerns can be addressed while an opportunity still exists to make changes.

Note: Thickness is not the only indicator of material cost. Other factors, such as number of plies used, material type, thickness tolerance, or the demand for this material may influence cost. **If no specific dielectric thicknesses are required, it is best to allow REYcomp to make the material selection. Materials that meet industry standards, are of lowest cost, and allow the most effective manufacturing methods will be utilized.**

3. Maintaining a balanced lay-up in relation to the Z-axis median of the board will assure minimum bow and twist. This balance includes the following:

   - Dielectric thickness of layer
   - Copper thickness of layers and its distribution
   - Location of circuit and plane layers



   A higher number of layers normally means an increase number of plane layers. Planes need to be balanced around the Z-axis median line of the lay-up, and ideally located internal to the board.

   If accepted Multilayer design rules are adhered to, boards will meet a maximum allowable bow and twist specification of 0.010 inch per inch (1%) or better.

4. Outer layer circuitry

   - Circuit area and distribution between the front and back of the board should be balanced as closely as possible.

   - Plating thieving of low pattern density of external plane area should be considered.

5. Thickness Tolerance

- As the overall thickness of a multilayer board increases, the thickness tolerance should also increase. A good rule is to specify a tolerance of +/- 10% of the overall thickness.

- **Always indicate where the thickness measurement is to be taken. Examples might be: glass to glass at rail guides, over gold contacts, over solder mask, etc.**

  When calculating the potential board thickness, consideration needs to be given to certain design characteristics. An example would be: Have the plane layers been pulled back from under the gold contacts? In that case, do not add the copper thickness of the planes to the board thickness, if measured across contacts.

NOTE: The contribution that the copper thickness of signal and plane layers make to the thickness of the board depends on the width and density of signal lines and the open area of planes. An isolated .006 inch line may totally embed itself into the prepreg and make no contribution to the thickness of the board. Talk with REYcomp if the overall thickness is of overriding importance. The needed overall thickness tolerance is primarily based on statistical material measurement data. The $\pm$ 10 % is a general recommendation. Depending on the multilayer lay-up structure and materials used, a closer tolerance is often achievable. Such a requirement needs to be discussed with REYcomp for appropriate focus.

Fabrication Drawing

The designer needs to specify the critical features of the design, i.e., finished board thickness, minimum dielectric spacing, number of layers and any electrical performance characteristic critical to the manufacture of the board, i.e., impedance requirements on the fabrication drawing. The fabricator should be left with the maximum amount of latitude the design will allow.

Section C: COMPLEXITY FACTOR CLASSIFICATION

Objective

To communicate rules and guidelines for the design of high density printed circuit boards using the “Complexity Factor Matrix" to ensure optimum manufacturability.

The "Complexity Factor Matrix" enables circuit board designers to assess the impact of a board's key characteristics on manufacturing. By understanding the Matrix and the rules and guidelines, one can improve board yield, which ultimately impacts quality, delivery, price, and environmental impact.

These parameters are preferred by REYcomp. Others may be considered but may result in lower yield and higher board prices.

Design For Manufacturing

Introduction

All new parts will be screened against the stated manufacturing capabilities either the first time they are built or whenever a change is made to the part number.

The Technical Support/Application Engineering group evaluates key design characteristics to determine what level of complexity a given board design represents.

The “Complexity Factor Matrix” has been developed to use as a tool in classifying parts. The matrix is structured with board characteristics located down the left-hand side, manufacturing areas impacted along the top, and the tolerances allowed for those characteristics are located down the right-hand side.

By using the matrix, one can make an initial assessment of the impact of a design’s characteristics on the manufacturing areas, and ultimately the price of the circuit board.

The following are definitions of the four major levels of complexity.

Board Producibility Levels

These levels reflect progressive increases in sophistication of design, tooling, materials and processing and, therefore progressive increases in fabrication cost. These levels are:

Class 1 General design complexity. Components typically placed on .100” grid. Designed trace width and spacing .007 inch or more.

Class 2 Moderate or standard design complexity. Components placed on .050 inch grid. Maximum of two traces between IC lands. Designed trace width and spacing .005 to .006 inch.

Class 3 High design complexity (surface mount pads of 0.020 inch pitch). Components placed on .050 inch grid, with traces and spacing .003 to .004 inch. This class may require special handling or process controls.

Class 4 These parts are outside our stated manufacturing capability. A quote and commitment for production is provided, once dedicated engineering resources are made responsible for the build of that part. The intent is to manage parts that are on the leading edge of our manufacturing capability through a progressive series of builds. As we gain experience, the end goal is a release for volume builds with predictable yields and the guarantee that customer needs and REYcomp commitments can be met.

Complexity Factors Matrix

June 1999

CATEGORY	INN	DRI	LAM	OUT	PLA	SM	FIN	DIMENSIONS
Trace Width	1			1				GE 0.007
	2			2				GE 0.004 & LT 0.007
	3			3		3		GE 0.003 & LE 0.004
	4			4		4		LT 0.003
Space Width	1			1				GE 0.007
	2			2				GE 0.004 & LT 0.007
	3			3		3		GE 0.003 & LE 0.004
						4		LT 0.003
Annular Ring Radius	1	1	1	1				GE 0.0085
	2	2	2	2				GE 0.005 & LT 0.0085
	3	3	3	3				GE 0.004 & LT 0.0065
	4	4	4	4				LT 0.004
Clearance Pad Radius	1	1						GT 0.0185
	2	2						GE 0.018
	3	3						GE 0.010 & LT 0.01375
	4	4						LT 0.010
Overall Profile Tolerance							1	GT ± 0.008
							2	GT ± 0.004 & LT± 0.008
							3	EQ ± 0.004
							4	LT ± 0.004
Finished Hole Tolerance								GE ± 0.003 HASL GE ± 0.002 No HASL
Finished Board Thickness								See page C-18
Aspect Ratio								See page C-19

Key:

INN ------ Inner Layer
DRI ------ Drilling
LAM ----- ML Lamination
OUT ----- Outer Layer

PLA ------ Plating
SM ------ Soldermask
FIN ------ Finishing (Profiling)
GT ------ Greater Than

GE ------ Greater Than or Equal To
LT ------ Less Than
LE ----- Less Than or Equal To
EQ ----- Equal To

Note: All dimensions are in inches

TRACE AND SPACE WIDTH (cont.)

GUIDELINES

Preferred Pad Construction for Class 2 6/6 Surface Mount Technology

Recommendations for one trace through 0.050 inch centered pads are as follows:

- Pad diameter 0.031 inch
- Hole callout 0.018 + 0.000/-0.018 inch; preferred drill diameter 0.018 inch
- Trace width 0.006 inch/Space width 0.006 inch
- These designs require 0.5‡ ounce outer layer copper foil construction for multilayers. Soldermask over bare copper is preferred. See Constraints page C-8.

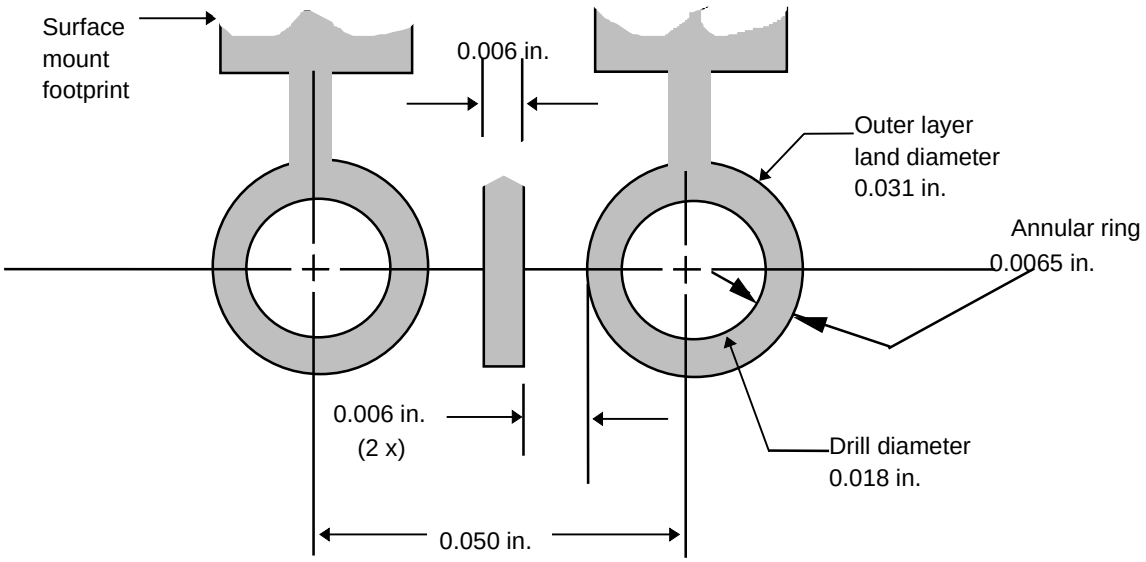


Figure 2 PREFERRED PAD CONSTRUCTION FOR 6/6 TECHNOLOGY

TRACE AND SPACE WIDTH (cont.)

GUIDELINES

Preferred Pad Construction for Class 3 5/5 Surface Mount Technology

Recommendations for two traces between 0.050 inch centered pads are as follows:

- Pad diameter 0.025 inch
- Hole callout 0.016 +0.000/-0.016 inch; preferred drill diameter is 0.0145 inch
- Trace width 0.005 inch/Space width 0.005 inch.
- These designs require 0.5‡ ounce outer layer copper foil construction for multilayers. Soldermask over bare copper is preferred. See Constraints page C-8.

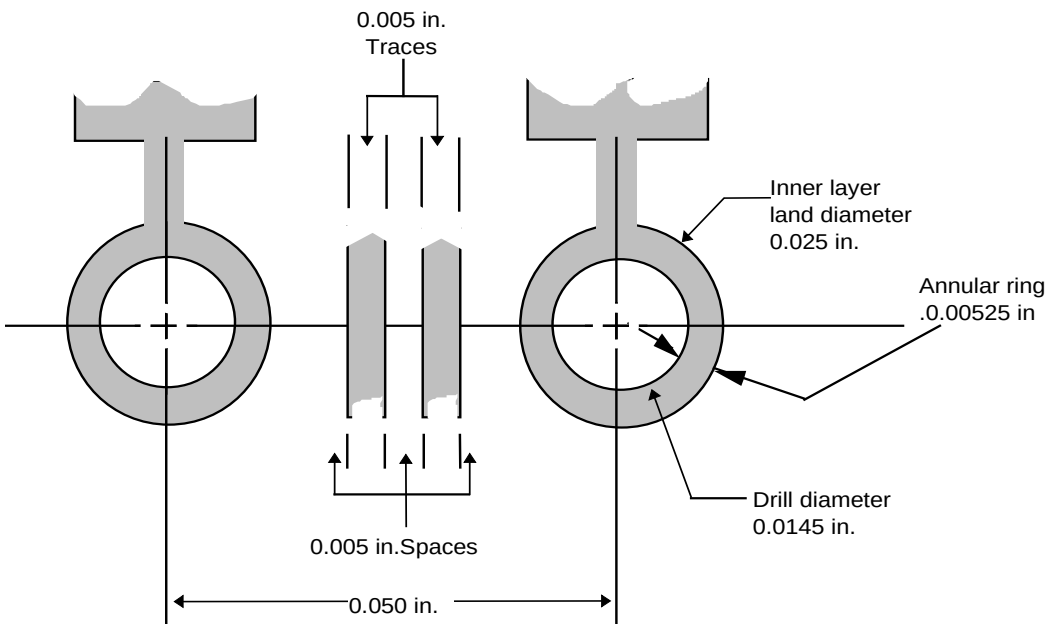


Figure 3 PREFERRED PAD CONSTRUCTION FOR 5/5 TECHNOLOGY

TRACE AND SPACE WIDTH (cont.)

GUIDELINES

Preferred Pad Construction for Class 3 4/4 Surface Mount Technology

Recommendations for three traces between 0.050 inch centered pads are as follows:

- Pad diameter 0.022 inch
- Hole callout 0.012 + 0.000/-0.012 inch; preferred drill diameter 0.012 inch
- Trace width 0.004 inch/Space width 0.004 inch

These designs require 0.5‡ ounce outer layer and inner layer copper construction for multilayers. Solder Mask over bare copper is preferred. See Constraints page C-8.

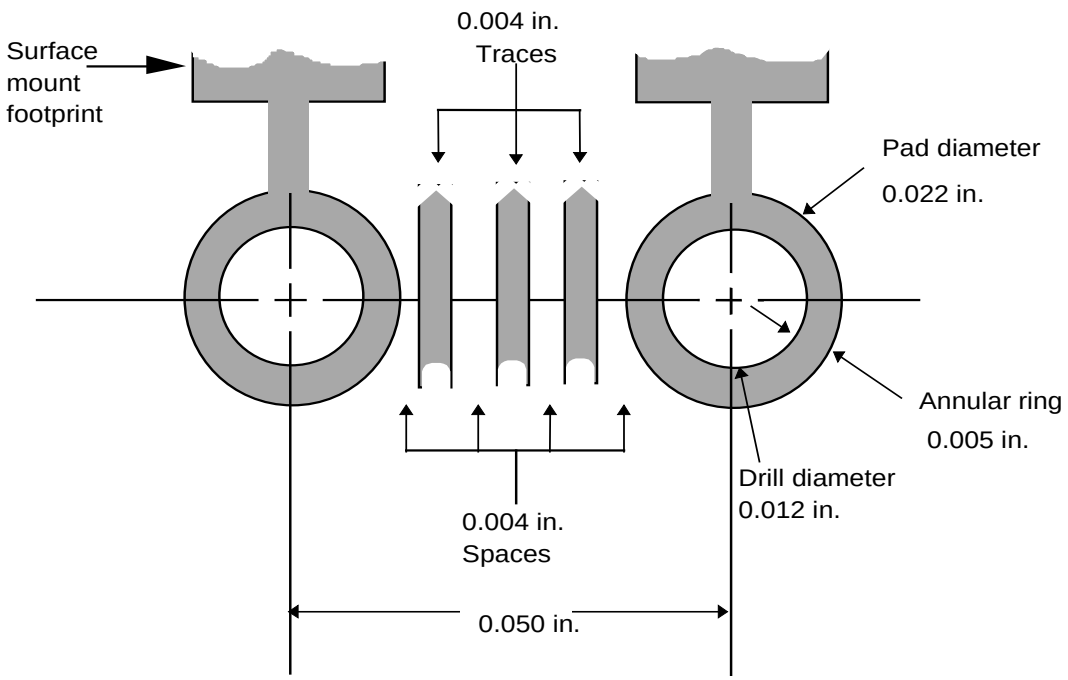


Figure 4

PREFERRED PAD CONSTRUCTION FOR 4/4 TECHNOLOGY

TRACE AND SPACE WIDTH (cont.)

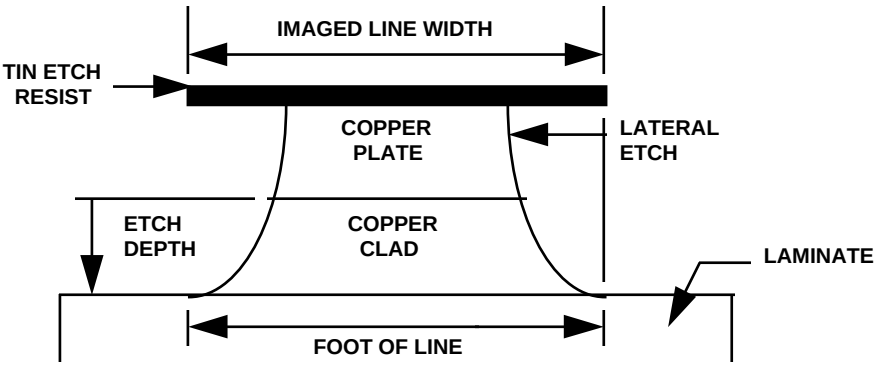
CONSTRAINTS

The trace width changes chiefly due to predictable losses during the etching process. The diagram below shows a cross sectional view of the inner and outer layer trace after etching.

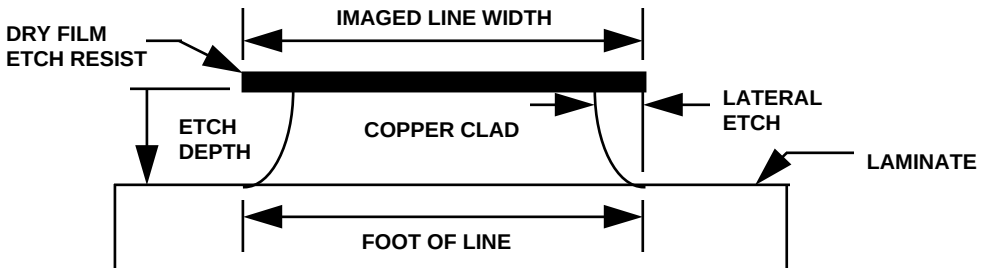
During the etching process, the etchant, due to impingement forces, removes copper downward and laterally. The tin etch resist in the case of outer layers and the dry film etch resist in inner layers, establishes the original line width, but cannot avoid eventual undercut of this boundary. For outer layer, by virtue of the additional electroplated copper, the effective ratio of vertical versus lateral etch is approximately 1:1. For inner layers the etch ratio is approximately 2:1. This leads to trace profiles as shown in the diagrams shown below.

Copper clad weight is the most important factor in controlling trace width. Using 0.5 ounce copper clad^{+} reduces the total copper thickness etched and thereby reduces the lateral etching.

The trace width is primarily controlled by the plotted trace width on the artwork. The etching process does not cause a significant change in the base line width (foot of line). The top of the line is reduced however. This is significant for electrical performance characteristics, such as impedance, since it reduces the cross sectional area and the effective (average) width of the line (see following page).



Outer Layer Line after Etching

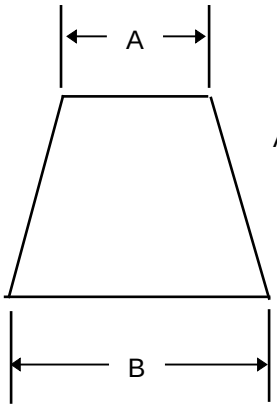


Inner Layer Line after Etching

Etch Factor

As the copper etches in the vertical direction, the lateral etch will reduce the top of the trace as indicated below (A). The nominal dimension of the foot of the trace (B) will remain representative of the plotted trace width.

Copper Weight Ounces (in.) [not including outer layer copper plating]	Total Lateral Reduction (top of line) A	Etch Factor (avg. reduction of line) A+B÷2	Estimated Line Width Tolerance
Outer Layers			
0.5 ounce copper (.0007) ‡	- .0014 inch	- .0007 inch	+/- .0008 inch
1.0 ounce copper (.0014)	- .0028 inch	- .0014 inch	+/- .001 inch
2.0 ounce copper (.0028)	- .0056 inch	- .0028 inch	+/- .0015 inch
Inner Layers			
0.5 ounce copper (.0007) ‡	- .0007 inch	-.00035 inch	+/- 0.0005 inch
1.0 ounce copper (.0014)	- .0014 inch	- .0007 inch	+/- 0.0008 inch



Averaging of Line Width:

$$\frac{A + B}{2}$$

Note: For purpose of averaging, the geometries of the line are considered to be trapezoidal.

As trace width and spacing decreases, especially below the 0.005/0.005 inch threshold, it becomes critical that 0.5 oz copper ‡ is utilized. Not only will thicker copper increase trace width tolerance and variation, but will also increase concerns about clearing of all copper between very close spaces.

Plated Finished Hole Tolerance

The finished plated hole tolerance as specified on the drawing.

RULES TO AVOID CLASS 4:

No tighter than +/- 0.002 inch on the finished plated hole size (complexity factor 3). Both finished hole size and tolerance become an issue when mixed technology (designs with both surface mount and through hole technology) is used on Hot-Air-Solder-Leveled boards. Holes which are drilled with less than a .024 inch drill may plug with solder.

CONSTRAINTS

Ability to control additive tolerances occurring in drilling, copper plating and Hot-Air-Solder-Leveling.

UNPLATED FINISHED HOLE DIAMETER TOLERANCES

Feature Size in Inches	Method	In Inches
0.033 to 0.063	Drill	± 0.001
0.064 to 0.200	Drill	+0.002/-0.001
0.201 to 0.266	Drill	± 0.002
> 0.266	Rout	± 0.005
> 0.266	Nibble Drill	± 0.003

Unplated Drilled Slot Size Tolerance

A slot feature is formed during the drilling process. A series of overlapping holes are drilled in a manner that produces a slot of variable length and width. These techniques are applicable to primary or secondary drilling operations. The slot length is controlled by the NC program and the slot width is established by the drill diameter.

Tolerances for length and width of slot

	Straight Slot (Non-Intersecting Slot)		**Intersecting Slot ('L' Slot, 'T' Slot, etc.)**	
	Length <= 2 x Width	Length > 2 x Width	Length <= 2 x Width	Length > 2 x Width
0.065" <dia	+/- 0.003"	+/- 0.002"	+/- 0.003"	+/- 0.002"
0.0453" <dia <=0.065"	+/- 0.006"	+/- 0.002"	+/- 0.006"	+/- 0.002"
0.031" <=dia <=0.0453"	**X**	+/- 0.003"	**X**	+/- 0.004"
dia <0.031"	**X**	**X**	**X**	**X**

Positional Tolerance

All Holes drilled at the primary sequence will be within 0.006 inch of diametrical true position. The hole location tolerance for those holes drilled at a secondary drilling operation is 0.014 inch true position referenced from a primary hole datum.

CONSTRAINTS

Secondary drilling through plated surface features produces burrs and results in excessive hand finish work.

Minimum and Maximum Drill Diameter

The minimum drill diameter is the smallest specified or selected drill diameter based on customer requirements. **Expense associated with drilling can be the second largest cost component of a printed circuit board.** Number of drill hits, stack height, and number of different drills selected are critical components of drilling. The number of boards that can be drilled in one set up (stack height) is determined by minimum drill diameter, registration tolerances, and board thickness.

RULES TO AVOID CLASS 4:

- No smaller than 0.008 inch diameter drill (for a finished plated hole tolerance of +.000\- 0.008 inch*). **Aspect Ratio must be taken into consideration when selecting minimum drill size.** See Page C19.

- Maximum hole size is 0.266 inch. Holes 0.153 or larger require pilot drilling.

CONSTRAINTS

The minimum drill diameter is determined by our plating capability. See Aspect Ratio Page C-19.

* Via holes of <0.021 drill diameter will probably remain plugged after HASL. No minus tolerance specified.

Drill Selection

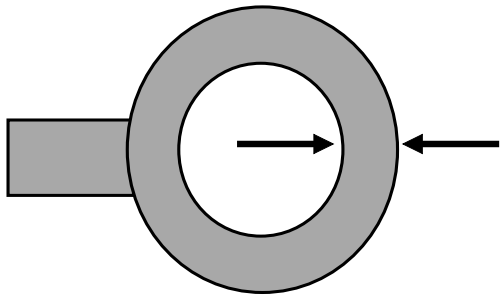
Available drill sizes are listed below. For holes plated with copper and hot air leveled, a drill size will be chosen that is 0.005 inch to 0.006 inch larger than the specified nominal finished hole size. For those holes which will only receive copper plating and organic coating, and no hot air leveled solder, a drill size will be chosen that is 0.003 to 0.004 inch larger than the specified nominal finished hole size.

Available Drills

(inches)	(inches)	(inches)	(inches)
.0087 90	.0610 1.55mm	.1160 32	.1820 14
.0100 87	.0625 1/16	.1181 3.00mm	.1830 4.65mm
.0120 83	.0635 52	.1200 31	.1850 13
.0135 80	.0650 1.65mm	.1220 3.10mm	.1875 3/16
.0145 79	.0670 51	.1240 3.15mm	.1890 12
.0160 78	.0689 1.75mm	.1250 1/8	.1910 11
.0180 77	.0700 50	.1260 3.20mm	.1935 10
.0200 76	.0709 1.80mm	.1280 3.25mm	.1960 9
.0210 75	.0728 1.85mm	.1285 30	.1990 8
.0225 74	.0748 1.90mm	.1299 3.30mm	.2010 7
.0240 73	.0760 48	.1319 3.35mm	.2031 13/64
.0250 72	.0768 1.95mm	.1339 3.40mm	.2040 6
.0260 71	.0785 47	.1360 29	.2055 5
.0280 70	.0810 46	.1378 3.50mm	.2090 4
.0292 69	.0820 45	.1405 28	.2130 3
.0310 68	.0827 2.10mm	.1417 3.60mm	.2165 5.50mm
.0320 67	.0846 2.15mm	.1440 27	.2188 7/32
.0330 66	.0860 44	.1457 3.70mm	.2210 2
.0350 65	.0866 2.20mm	.1470 26	.2264 5.75mm
.0360 64	.0890 43	.1495 25	.2280 1
.0370 63	.0906 2.30mm	.1520 24	.2323 5.90mm
.0380 62	.0925 2.35mm	.1540 23	.2340 A
.0390 61	.0935 42	.1555 3.95mm	.2362 6.00mm
.0400 60	.0945 2.40mm	.1570 22	.2380 B
.0410 59	.0960 41	.1590 21	.2402 6.10mm
.0420 58	.0980 40	.1610 20	.2441 6.20mm
.0430 57	.0995 39	.1634 4.15mm	.2460 D
.0453 1.15mm	.1015 38	.1654 4.20mm	.2480 6.30mm
.0465 56	.1024 2.60mm	.1660 19	.2500 1/4
.0472 1.20mm	.1040 37	.1673 4.25mm	.2520 6.40mm
.0492 1.25mm	.1065 36	.1695 18	.2559 6.50mm
.0512 1.30mm	.1083 2.75mm	.1719 11/64	.2570 F
.0520 55	.1094 7/64	.1730 17	.2610 G
.0531 1.35mm	.1100 35	.1752 4.45mm	.2638 6.70mm
.0550 54	.1110 34	.1770 16	.2660 H
.0571 1.45mm	.1122 2.85mm	.1800 15	
.0595 53	.1130 33	.1811 14	

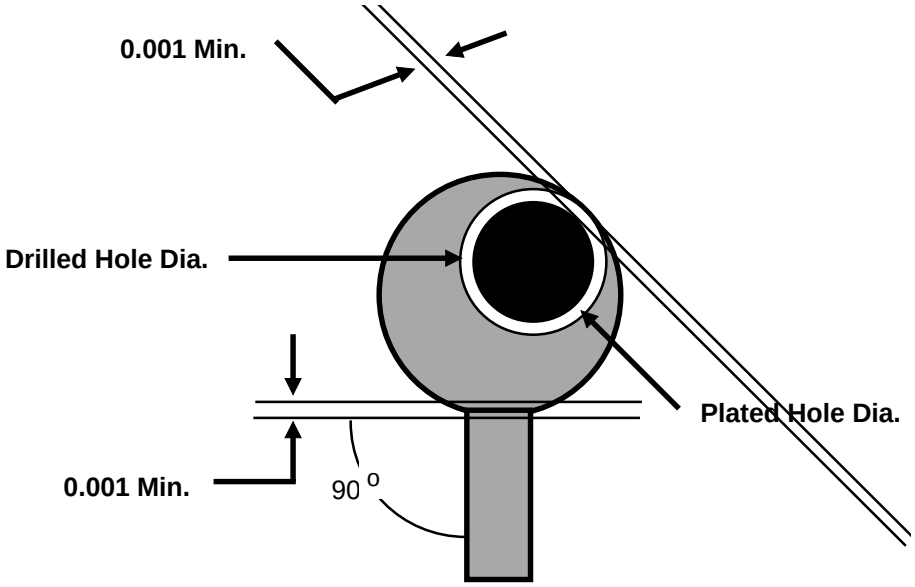
Annular Ring

The difference between the drill diameter and the corresponding circuitry pad diameter as measured on the master artwork divided by 2.



RULES TO AVOID CLASS 4:

Pads on all circuitry artwork must be 0.008 (2 x 0.004) inch larger than the drilled hole to ensure 0.001 inch minimum annular ring on the finished product. In this case the drilled hole wall will be tangent to the edge of the circuitry pad. See diagram below. The plating in the hole wall (typically 0.001 inch) will be included in the measurement of the finished product. Any annular ring requirement specified as larger or excluding the plating in the hole wall will require a larger circuitry pad and/or smaller drill size.



CONSTRAINTS

Material stability during processing, especially multilayer lamination, photo tool stability and drilling accuracy.

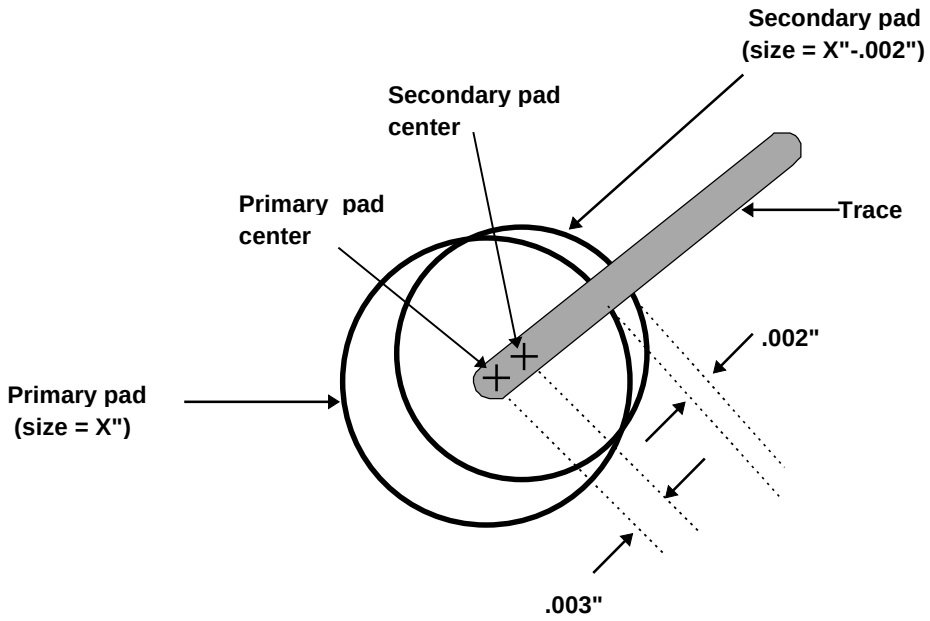
Tear Drop Pads

This process is designed to provide additional metal at the critical junction of a pad and a run. When an order is drilled and misregistration occurs, it has been theorized that a long-term reliability issue can arise if the misregistration occurs at the junction of the pad and the trace. Adding metal at this location helps ensure that an adequate connection is made and maintained.

The tear dropping process involves adding secondary pads at the junction of an existing (primary) pad and a circuit run. These secondary pads are sized 0.002 inch smaller than the primary pads, and the center is placed 0.003 inch away from the center of the primary pad.

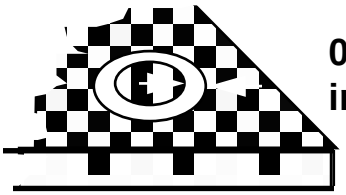
This tooling process is conducted using IPC standards for tear dropping and has proven to be highly reliable and effective.

TEAR DROP ILLUSTRATION



Clearance Pad

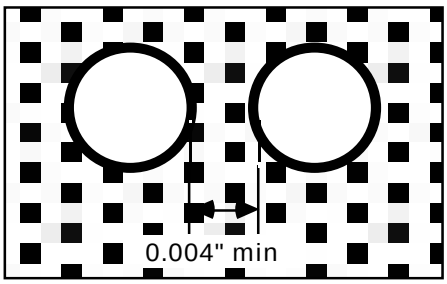
On ground and power planes the clearance pads are the inner layer areas free of copper surrounding the finished hole diameters. It is calculated by measuring the difference between the specified drill diameter and the corresponding clearance pad diameter as measured on the master artwork and dividing by 2.



RULES TO AVOID CLASS 4:

- To ensure a minimum of 0.005 inch clearance between the plated hole and the edge of the clearance pad, a clearance pad 0.020 (2 x 0.010) inch larger than the drilled hole must be provided on the artwork. Please refer to IPC-D-949 Design Standard for Rigid Multilayer Printed Boards for specifics.

- If the plane layer design leaves strips of copper between clearance pads, a minimum of 0.004 inch is required between clearance pads to avoid causing shorts due to resist lifting and redepositing. (Again as measured on the master plotted artwork.)



CONSTRAINTS

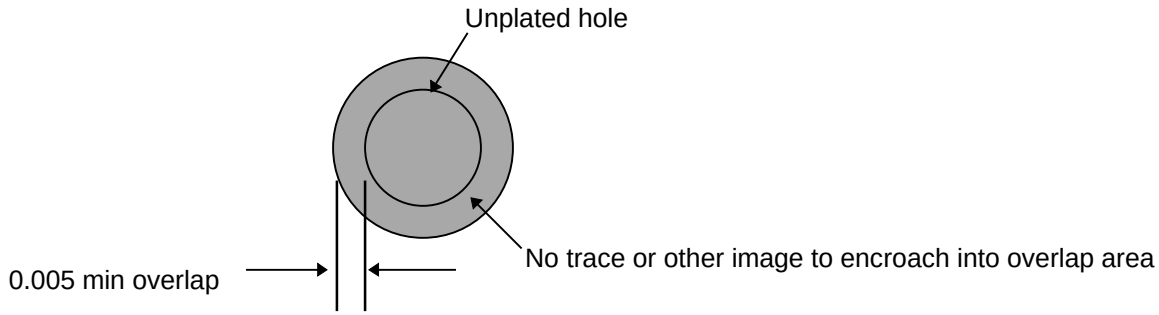
Material stability during processing i.e. multilayer lamination; photo tool stability; and drilling accuracy.

Tenting of Unplated Holes

For improved locational accuracy of unplated holes, it is preferred to drill them during the initial plated through hole drilling setup. In order to avoid plating of etch resist into these holes, it is required that the unplated holes be tented with dry film during the outer layer imaging process, overlapping the hole edge for a minimum of 0.005 inches. Before the etching process, this tent is removed. This allows the removal of copper from the hole walls during the consequent etching process. The designer needs to follow these guidelines:

Maximum hole diameter to be tented = 0.200 inch

Minimum overlap required around unplated hole = 0.005 inch radius larger than hole.



Summary Of Hole To Pad Relationships

The relationship between the finished hole size and the pad sizes used in a design is critical to the manufacturability and reliability of a circuit board. To assist in understanding this relationship, a summary of information is presented on previous pages follows.

RULES TO AVOID CLASS 4:

No circuit pads with less than 0.004 inch annular ring (0.008 inch larger than the drill diameter) unless pad breakout is allowed. If less than 0.005 inch annular ring is required, then tear dropped pads are recommended.

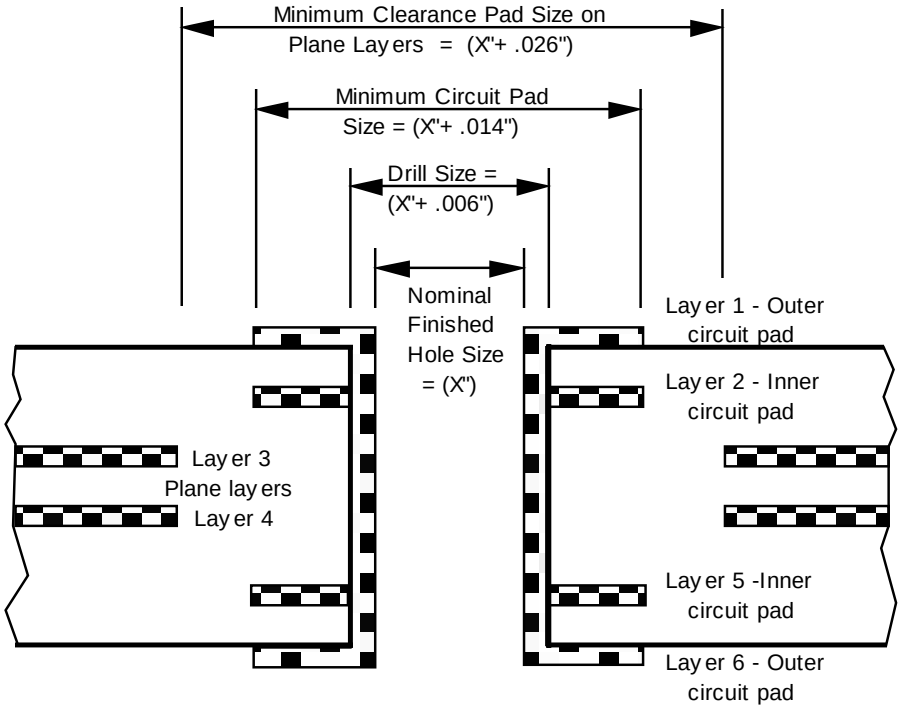
No clearance pads on plane layers with less than 0.010 inch annular ring (0.020 inch larger than the drill diameter).

Design For Manufacturing

GUIDELINES: (See illustration below)

The drill size for plated holes is 0.005 inch to 0.006 inch larger than the specified nominal finished hole size. This is dependent on drill sizes available. The drill size for unplated holes is the size closest to the specified nominal finished hole size as possible. This is dependent on the drill sizes available.

To avoid breakout, circuit pads must be 0.008 inch larger than the drill size (this equates to .014 inch larger than the specified nominal finished hole size). To maintain a minimum 0.005 inch dielectric space between the hole wall and the edge of a plane layer clearance, the clearance pads must be 0.020 inch larger than the drill diameter (this equates to 0.026 inch larger than the specified nominal finished hole size for plated holes).



Finished Board Thickness

The maximum finished board thickness measured copper to copper. This measurement is critical to the fabricator as it affects aspect ratio, drilling and profiling stack heights, and fixed limitations of processing equipment. For additional information please refer to the Materials Section.

GUIDELINES:

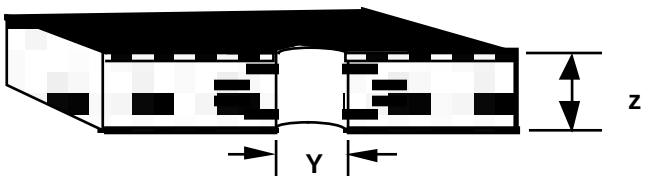
- The overall board thickness including soldermask must be between 0.020 inch and 0.270 inch.

CONSTRAINTS

Plating racks, Electroless baskets, U.L. Flammability rating, Outer Layers scrubbers, laminators. Boards less than 0.052 inch require special handling and processing at the Hot-Air-Leveling operation, which negatively affects machine capacity and affects cost.

ASPECT RATIO

The **maximum** board thickness divided by the **smallest** selected drill diameter. The maximum board thickness is the calculated thickness over copper before plating. Additional thickness caused by plating, hot air solder leveling, or soldermask has no impact on aspect ratio.



RULES TO AVOID CLASS 4:

See Matrix on Page C-19

Aspect Ratio Plating Capability

Drilled Hole Size (inch)	Board Thickness (inch)/Aspect Ratio			
	0.070	**0.093**	**0.125**	**0.265**
0.065	OK	OK	OK	4.1 : 1
0.045	OK	OK	OK	5.9 : 1
0.035	OK	OK	OK	7.6 : 1
0.025	2.8 : 1	3.7 : 1	5.0 : 1	10.6 : 1
0.020	3.5 : 1	4.65 : 1	6.25 : 1	13.3 : 1
0.018	3.9 : 1	5.1 : 1	6.9 : 1	14.7 : 1
0.016	4.4 : 1	5.8 : 1	7.8 : 1	
0.0135	5.2 : 1	6.8 : 1	9.3 : 1	
0.0125	5.6 : 1	7.4 : 1		
0.010	7 : 1	9.3 : 1		

Note: This Aspect Ratio Matrix provides general guidelines for establishing aspect ratio capability. If board thickness and minimum drill size vary considerably from above data, please contact REYcomp.

Overall Finished Profile Tolerance

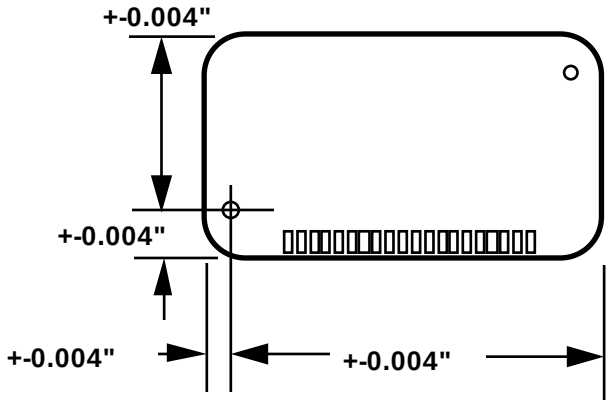
The finished board profile dimensions and tolerances as specified on the drawing.

RULES TO AVOID CLASS 4:

The overall dimensional tolerance is no less than +/- 0.004 inch from drilled datum hole to any profiled board edge. Per IPC-D-300: "One board edge should be located from a datum, and where applicable other edges should be dimensioned from that same datum. Where board outer edges have a relationship to each other they shall be dimensioned using a single dimension to maintain that relationship."

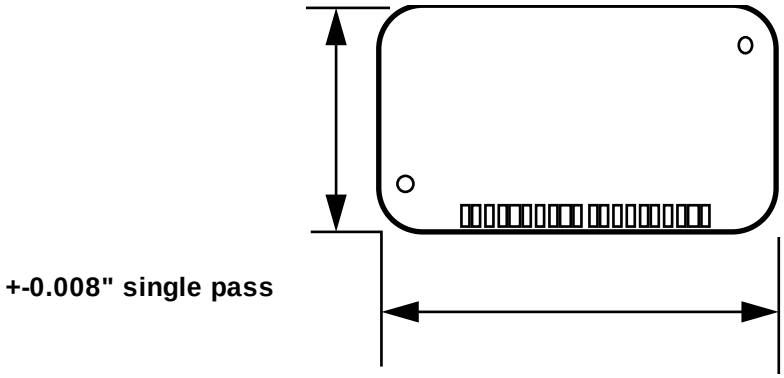
Design For Manufacturing

DATUM TO EDGE



Board edge to edge tolerance should be no less than +/- 0.008 inch. Internal routed features such as holes shall have tolerances of no less than +/- 0.005 inch across the feature edges. If closer tolerances are required, a special process needs to be negotiated with our manufacturing engineers.

EDGE TO EDGE



GUIDELINES

X/Y AXIS PROFILING

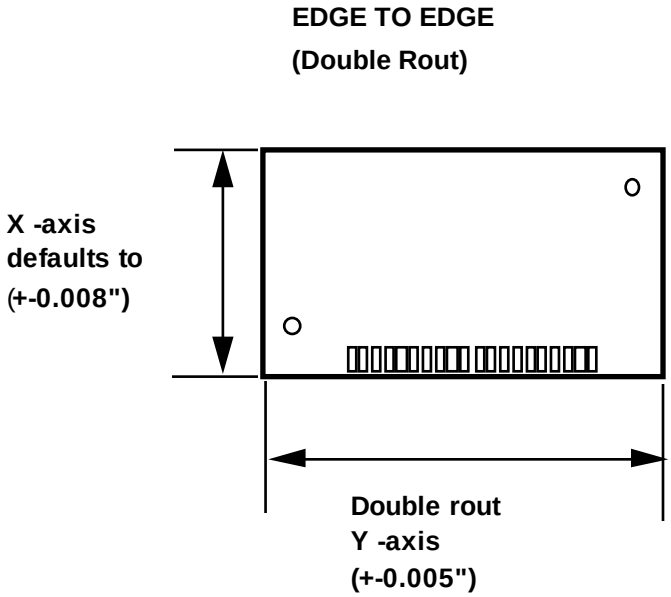
Use the most generous tolerance that the product will allow to minimize board price. Additionally, use only one cutter size. The preferred cutter size for routing is 0.125 inch or 0.093 inch diameter. Avoid use of smaller cutters.

Avoid routing through metal features. The result requires excessive hand de-burring and can cause quality defects.

SPECIAL TIGHT TOLERANCE PROFILE PROCESS:

Double routing of **internal features** (holes or cutouts) can be applied in any axis. Tolerance shall be no less than +/-0.004 inch across routed edges of the feature.

Double routing of **external features** can be performed in one axis of the circuit board only due to material and tooling stability. Tolerance shall be no less than +/- 0.005 inch from feature edge to feature edge in the double rout axis. The opposite axis defaults to +/- 0.008 tolerance.



CONSTRAINTS

Accuracy of routing operation and most importantly capacity.

Our standard cutter sizes produce the following radii 0.062 inch, 0.047 inch, and 0.031 inch = .062 inch cutter.

Conventional pin routing requires a minimum of two pins per board. Pin sizes to be greater than 0.062 inch and less than 0.251 inch.

Tab Routing

The preference is to set up parts for tab routing as a function of the tooling operation. To avoid unnecessary modifications to the mechanical drawing, it is preferred that customer provide only a note stating that the part needs to be shipped in panel form, delta notes indicating where tabs cannot be located. If the location of the parts in the panel is critical, the dimensions of the datums of the parts to the component assembly locating holes must be provided.

The following are the parameters used in setting up a tab routed panelized part:

- Locate tabs .350 inch minimum from any board corners.
- Place tabs .350 inch minimum from any board corners.
- Place tabs .350 inch minimum from datum holes, or directly on center.
- A .125 inch cutter will be utilized, unless design requires otherwise. All cut paths that are not between boards will be .125 inch wide; preferred spacing between boards is .250 inch, .150 minimum.
- Place tabs 3.00 +/- .50 inch apart from each other.
- Keep tabs in a straight line with X - Y axis if possible.
- Where there are component holes or traces close to the board edge, try to avoid tabbing in these areas to prevent the traces or hole walls from fracturing.
- Tab width is .125 +/- .010 inch.
- Tab location dimension is +/- .025 inch.
- Dimension tabs to the center of the tab on a .025 grid.
- Place tabs .250 +/- inch minimum away from any radius on the outside board edge.

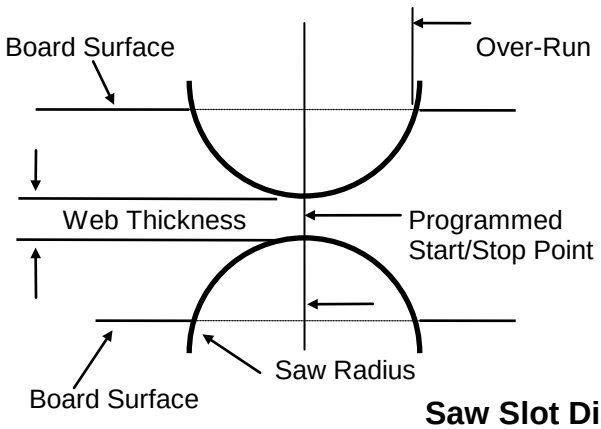
Scored Board Profiling

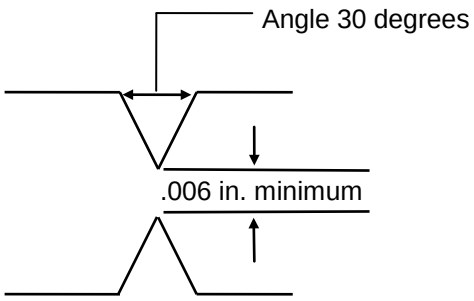
This process places grooves on opposite sides of a panel or between boards, for the purpose of depanelizing by snapping the boards from the panel. Since boards can be "butted up" against each other, more boards may be placed on the panel‡ thereby reducing the cost of the board.

Design Guidelines

Score locations need to be clearly identified on the drawing, with centerline of groove-feature referenced.

- The web thickness (material remaining between opposing grooves) must be specified. Typical web thickness is 0.008 inch to 0.014 inch. Minimum web thickness is 0.006 inch. A different web thickness may specified within a panel, but not within a single score cut.
- The groove angle need not be specified. It is fixed at 30 degrees.
- The depth of the groove should not be specified, because it is not controlled (the web thickness is controlled). Also, the centering between top and bottom should not be specified.
- To facilitate depanelization, grooves running to the edge of the panel are recommended.
- The groove width for a typical 0.062 inch board with a 0.012 inch web is about 0.020 wide at the surface of the board. Image features need to be pulled back a minimum of 0.040 inch from the score line center (image edge) for this board and web thickness.
- Overall board thickness suitable for scoring is 0.030 inch to 0.125 inch.





Saw Slot Diagrams

Achievable Tolerances:

Web Thickness	+/- 0.002 inch
Edge to Edge	+/- 0.005 inch
Datum to Edge	+/- 0.008 inch

CONSTRAINTS

- Diagonal scores or curved scores are not possible. Scores must be parallel to edge of panel.
- The circular 4 inch diameter saw blade causes an over-run at the ends of each cut. For a typical 0.062 inch board with a 0.012 inch web, this over-run amounts to approximately 0.3 inch. The distance between boards on a panel must compensate for this, if the boards are offset on the panel.
- Because of problems associated with stacked tolerances in conjunction with multiple set-ups, it is not recommended to have both scoring and profile routing on the same panel.
- With the exception of panel borders, scoring should not cut metal.

For special requirements please contact REYcomp.

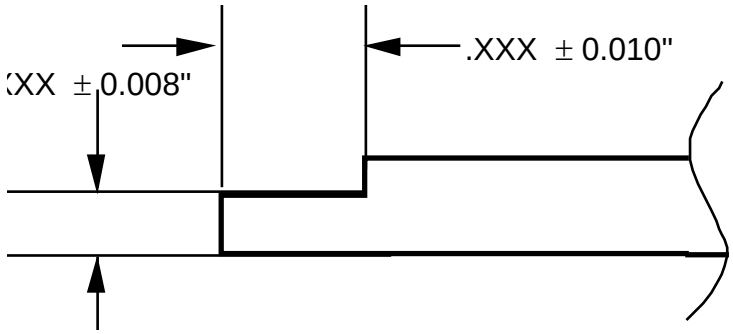
Hand Finishing Operations

MANUAL EDGE MILL

Boards may require edge milling to reduce the circuit board thickness to a specified thickness and tolerance. Typically this is done to allow the board to fit into a card guide when assembled.

The milled edge is usually a "step" at the edge of the board. See diagram below. The depth of the step is variable from 0.010 inch removed to 0.032 inch remaining. The width of the step is variable from 0.020 inch to 0.375 inch. Milling requirements should be limited to simple cuts i.e. two straight edges and simple corners. The path of the mill is limited to 90 degree turns and internal radii are controlled by cutter diameter (minimum 0.125 inch and common standard sizes). Geometries other than a step are possible but need to be evaluated on an individual basis as processing time is prohibitive. **Double sided milling is strongly discouraged as edge thickness accuracy is reduced.**

The finished thickness of the milled edge can be held to +/- 0.008 inch for a single sided milled edge. For a double sided milled edge the finished thickness can be held to +/- 0.010 inch. The width of the step can be held to +/- 0.010 inch.



Internal tooling pins are required. These tooling holes must be internal to the finished board and should be located as close as possible (but not actually in) the portion of the board to be milled. The finish produced by the mill process is similar to that produced by NC edge profiling. No fractured glass fibers are produced.

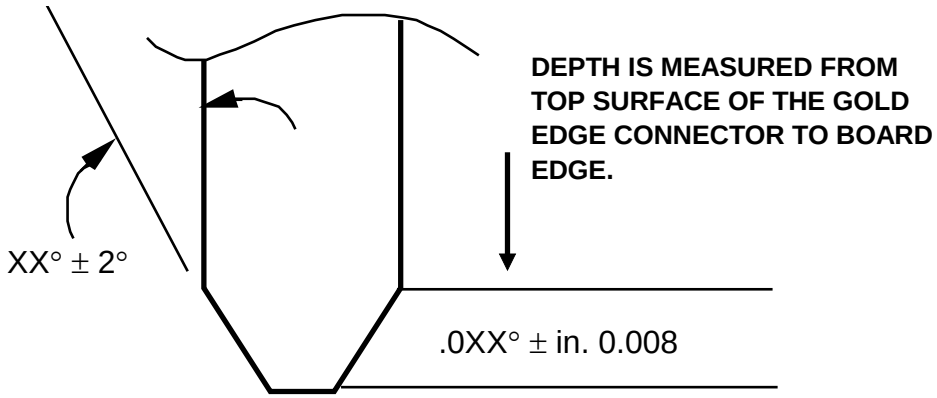
Edge Bevel

Edge beveling may be performed on the outer edge of the board, a recessed segment of the board, or internal to the board. Inner layer plane layers must be recessed to avoid exposing the plane when the boards are beveled. The following angles and depths may be achieved given sufficient board thickness:

20 degrees by **0.070** inch depth

30 degrees by **0.050** inch depth

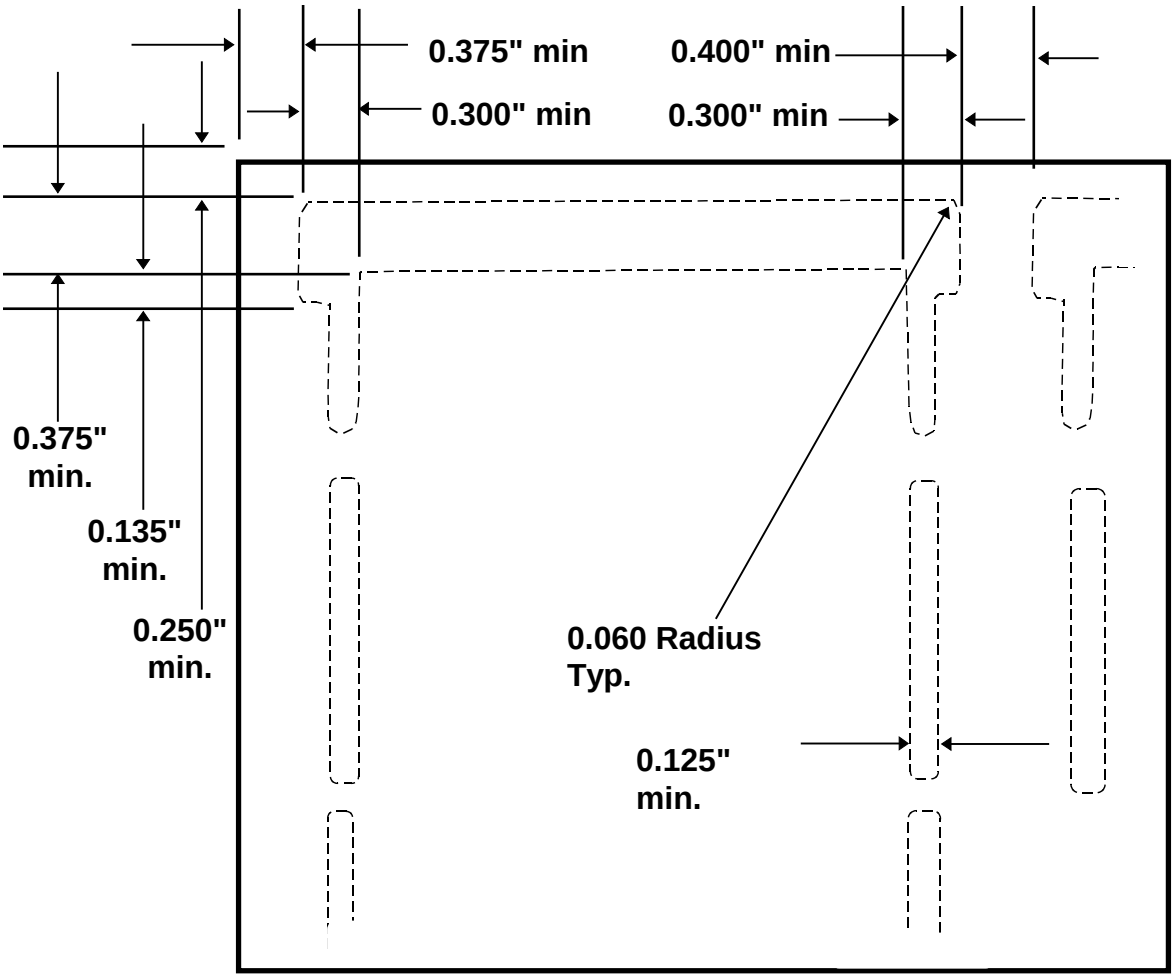
45 degrees by **0.040** inch depth



Design For Manufacturing

Please refer to the diagram below for dimension requirements for bevels performed internal to the flat.

DIAGRAM OF DIMENSIONS REQUIRED FOR INTERNAL EDGE BEVEL



Section D: PLATING OPTIONS

For plated-through-hole circuit boards, electroless copper, followed by electro-plated copper is deposited onto the hole wall to an average thickness of .001 inch. During the copper electro-plating process, external lines receive an average of .0013 inch copper plating, in addition to the original 0.5 or 1 oz copper foil already present.

All exposed circuitry, depending on specifications either before or after soldermask, needs to be protected by one of the finishes identified below.

Nickel -Matte Tin

- Typical thickness: 300 μinch Tin over 200 μinch nickel.
- Solderable surface
- Good shelf life

Nickel - Hard Gold

- Typical thickness: 30 to 50 μinch gold (99.7%) over 200 μinch nickel or 8 to 12 μinch gold (99.7%) over 200 μinch nickel for a solderable surface
- Excellent corrosion resistance
- 130 to 220 Knoop hardness
- Excellent wear resistance, best for surface rotary switches, on-off contacts, and edge connectors
- Excellent shelf life

Nickel - Soft Gold

- Typical thickness: 30 to 50 μinch gold (99.9%) over 200 μinch nickel
- Excellent corrosion resistance
- Less than 90 Knoop hardness
- Good for pressure contacts and aluminum or gold-wire bonding
- Fair wear resistance
- Excellent shelf life

Electroless Nickel/Immersion Gold (99.9% Gold)

- Typical thickness: 3 to 8 μinch gold over 180 μinch nickel
- Excellent corrosion resistance
- Good for aluminum wire bonding
- Excellent for fine-pitch technology
- Excellent solderability
- Excellent shelf life

HASL (Eutectic: 63% Tin - 37% Lead)

- Typical coating thickness: 30 μinch to 200 μinch, design dependent.
- Excellent solderability
- 0.025 inch pitch capability
- 0.030 inch minimum board thickness capability
- Good shelf life

Organic Solderability Preservative (OSP) or Anti-tarnish‡

- Typical coating thickness: 8 μinch to 20 μinch
- Excellent solderability
- Excellent surface coplanarity and hole size uniformity
- Excellent for use in fine-pitch technology
- Improved surface contrast - assembly vision capability
- Board not subjected to thermal shock (as with HASL)
- Good shelf life (12 months)

Gold Plating

OBJECTIVE

To communicate rules and guidelines for the design of gold contact areas on high density printed circuit boards. By understanding the processing constraints of the double image processes the circuit board designer can have a positive influence on the board price.

Selective or Double Image Plating

This process is reserved for parts that have requirements for gold areas internal to the board. It requires the extra labor and materials associated with double image plating.

Design Constraints

The tin image should include all the plated area excluding that called out to be gold plated (tin plating should not overlap into the gold plated area). The gold image should include all of the area designated to be gold plated on the drawing.

The gold image overlap into the tin area is between 0.050 to 0.100 inch.

In the double image area, holes must be supported with pads on both sides having the same type of plating, either tin or gold. If it is necessary to plate both gold and tin in the same hole, then a breakout pad must be provided within the tin film on the opposite side of the standard pad. If a hole is required to be gold plated, then the minimum copper thickness requirement in this hole must be waived.

Internal finger contacts, when called out to be gold plated, should include the entire contact area.

The trace width in the overlap area must be 0.010 inch minimum.

The spacing between parallel runs or pads within the overlap area should be greater than 0.015 inch. If the spacing is less than 0.015 inch, then the overlap must be staggered by 0.020 inch minimum.

Edge Connector Plating

The preferred manufacturing process for gold plating of edge connectors is tab plating. This process does not require the extra labor and materials associated with double image plating.

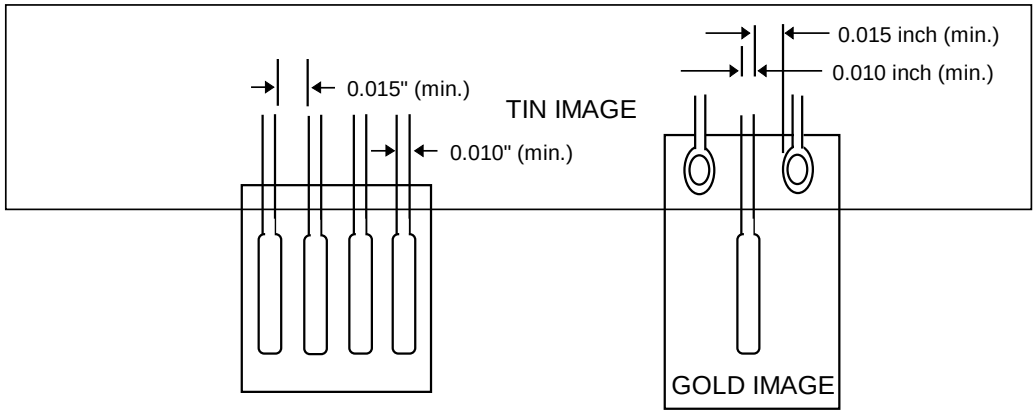
Design Constraints

- The maximum length of the gold plated tab is plated 0.8 inch.
- The maximum plating depth is 2.5 inches from the shear line (see diagram on next page).
- A minimum distance of 0.030 inch between contact pads allows good plating tape adherence and a well defined line between the gold plated area and the solder coated area.
- The annular ring of a through hole must be a minimum of 0.030 from the edge of the gold plated area to prevent “black holes”, resulting in solderability problems. It is best to keep holes as far away as possible from the gold edge connector area.

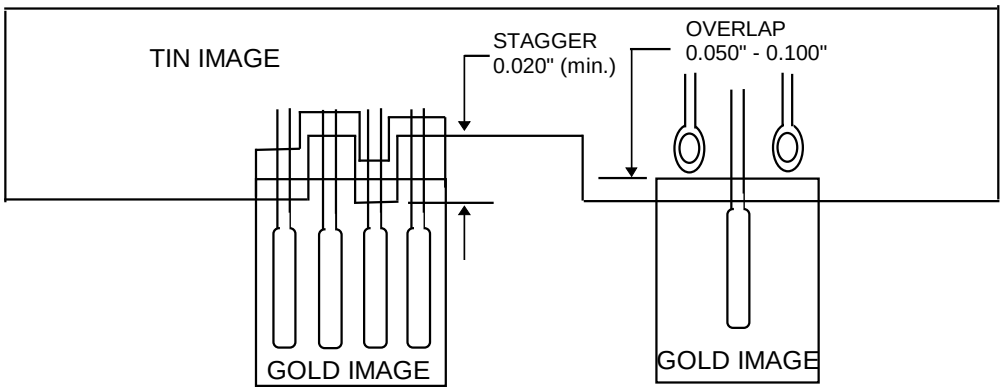
Note: The tab plate process is not set up for through hole plating. It is a surface plating process. Gold over nickel plating of the hole wall would be unreliable.

Design For Manufacturing

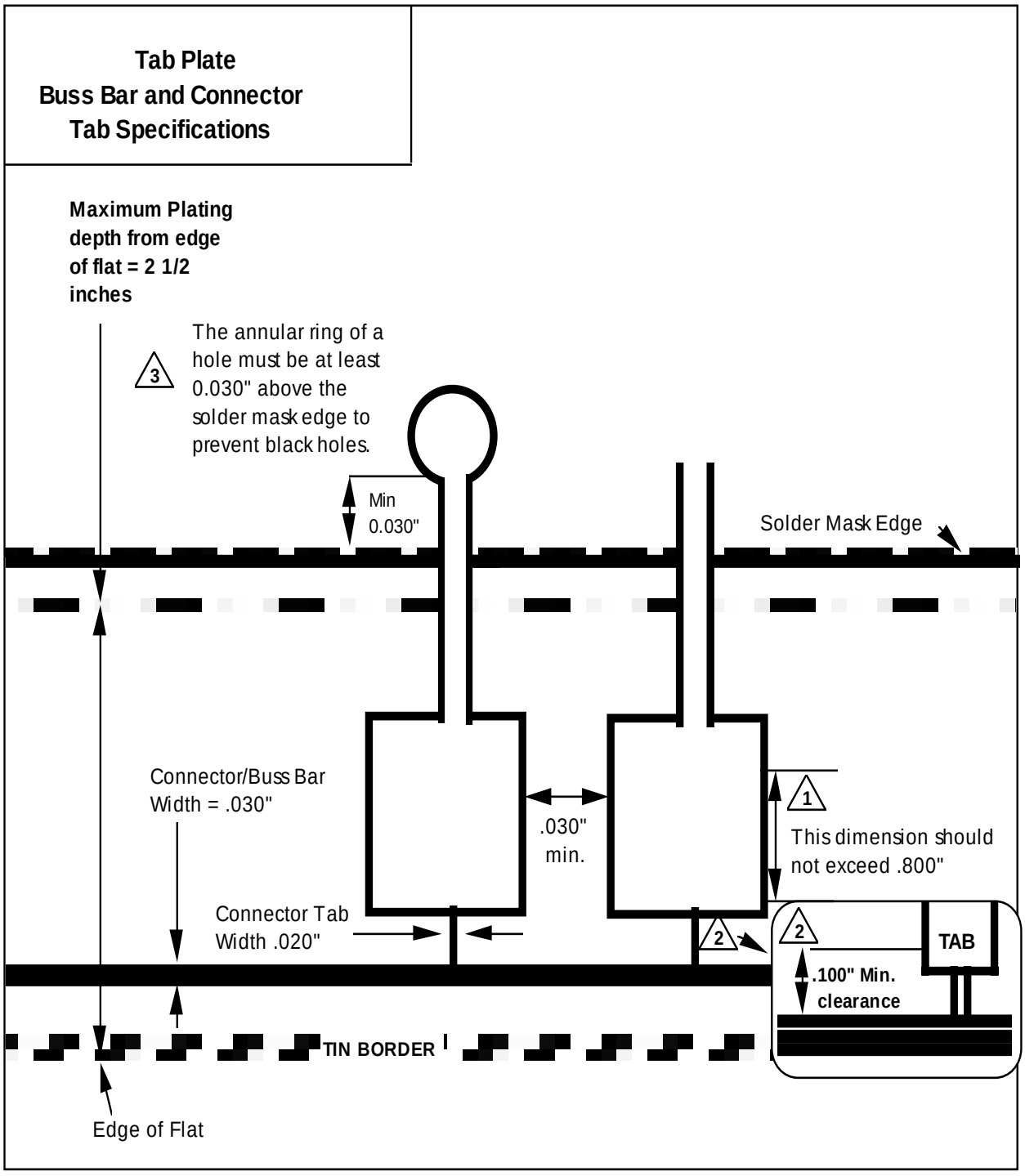
SELECTIVE PLATE FILM



PREFERRED SELECTIVE PLATE FILM



Design For Manufacturing



Section E: **SOLDERMASK**

Objective

To communicate rules and guidelines for designing soldermask artwork based on mask type.

Soldermask Availability

A variety of soldermasks have been selected to fill the needs of our customers. The following is a description of the soldermasks currently available. The need for closer tolerances has driven the implementation of photo-imageable soldermasks.

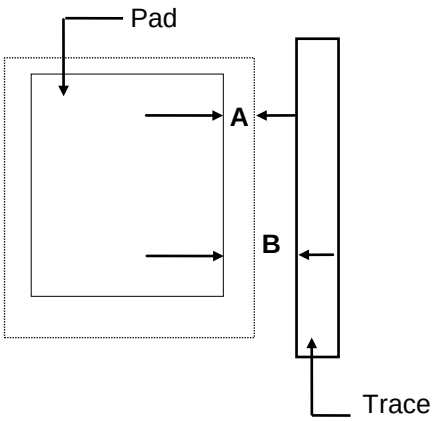
Liquid Photo-Imageable (LPISM) Soldermasks

Enthone DSR 3241 ‡ is applied using the flood screen coating process, while PROBIMER 52M® is applied via the curtain coating process. Enthone DSR 3241 has a green semi matte finish. Enthone DSR 3241soldermask has improved resolution capability, meaning that it can hold a finer feature, such as a "dam" between SMT pads. Liquid Photo-imageable soldermasks are considered to be soldermasks of choice for most circuit board product due to their high resolution, excellent electrical properties and compatibility with surface mount technology.

Hole "tenting" is available through the via-cap process in which PC401®, a thermally cured epoxy, is screened over the holes to be tented, after liquid photo-imageable soldermask is applied. This is an advantage for vacuum applications after assembly.

Soldermask Design Constraints, General

- The customer should provide master pad soldermask files, i.e. soldermask pads should be the same diameter as the outer layer pads. Modifications, to provide the correct clearance pad sizes necessary for processing, are performed as part of the initial tooling process. These clearance pad sizes result in no encroachment of the soldermask on the pads.



	A Minimum S/M Clearance per Side (mils)	**B** Minimum Spacing Pad to Trace (mils)
Nomenclature	10	**---**
Screened Requirements	7	**---**
Enthone DSR 3241	2*	5*

* IPC A600 Rev E Class II and III acceptance requirement

Note: Minimum spacing between pad and trace (B), if less than required, will result in either solder mask on pad or exposed metal on trace.

- Hole Clearing

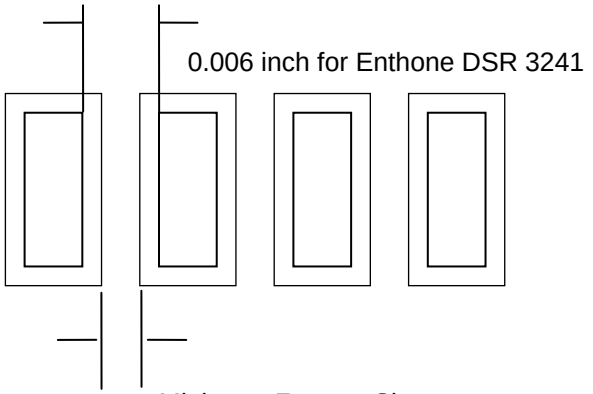
  With Enthone DSR 3241 , in cases of holes ≤ 0.018 inch and 0.003 inch dams (see following page), holes may remain plugged due to special process requirements. With normal processing, holes ≤ 0.0135 may remain plugged.

- Adhesion of Soldermask (“Dams”) between SMT pads

  If a small soldermask feature is required between closely spaced pads, two items are critical, the Minimum Spacing that is provided between pads, and the Minimum Soldermask Feature size that can be successfully reproduced. These dimensions are as follows:

Design For Manufacturing

Minimum pad spacing



Minimum Feature Size

0.002 Inch for Enthone DSR 3241

Note: If pads are closer than the minimum spacing described above, areas between pads should be free of soldermask, or the hold-down reliability will not be 100%.

The strength of soldermask adhesion over gold plating depends on the type of soldermask, type of gold, and the end-user processing conditions. It is recommended that the designer contact REYcomp before finalizing design.

Tenting of Via Holes with Soldermask

Via Capping with Screened Resist

Hole capping is available through the Via Cap process. On boards coated with liquid photo-imageable mask, the vias can be screened with soldermask creating an epoxy cap. Artwork modifications necessary for processing are performed as part of the initial tooling. A separate design file must be provided by the customer, which includes only those vias which are to be capped. The customer needs to provide master pad soldermask and via files, i.e. soldermask and via pads that are the same size as the outer layer pads.

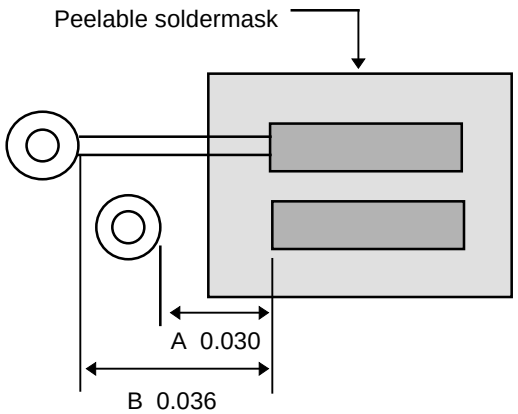
Via Capping Design Constraints

- The maximum finished hole size for via capping is .020" diameter (preferred drill diameter 0.021 inch).
- Generally, the non-test vias are capped on the bottom side of the board. Via capping on both sides results in raised or broken caps. Therefore, it is not permissible.
- Via caps will have a raised surface of about 0.0024" +/- 0.002" inch above the outer layer copper pad. This measurement may include solder and/or permanent soldermask thickness.
- REYcomp will guarantee a minimum of 98% of holes plugged, with open holes randomly located.

Peelable Soldermask

Peelable soldermask (PSM) is a temporary soldermask which is selectively applied to a circuit board prior to the Hot Air Solder Leveling (HASL) process. Its purpose is to protect gold plated surfaces from being coated with solder. After the HASL process, the PSM is removed manually.

A = Minimum distance between a gold contact and a gold feature or unplated hole.
B = Minimum distance between gold contact and a connected copper feature



Peelable Soldermask design requirement

Peelable Soldermask Constraints

- If PSM terminates in the bare glass areas around pads (or other areas not covered with permanent mask), it will leave a blue residue in those areas.
- A maximum of 24 individual strips of PSM is allowed per panel. This is to minimize the time required to manually peel PSM strips from panel.
- The permanent soldermask file must provide a minimum coverage of the copper/gold interface (see drawing).

It is recommended that the designer discuss PSM requirements with REYcomp before finalizing design.

NOMENCLATURE

- Letter size: ≥ 0.006" Line Width, ≥ 0.035" Height.
- Color: White preferred; Yellow, Orange and Black also available.
- Nomenclature over Solder (HASL) will have poor adherence.
- Nomenclature placed over bare copper before HASL will have an apparent copper "halo" after the HASL

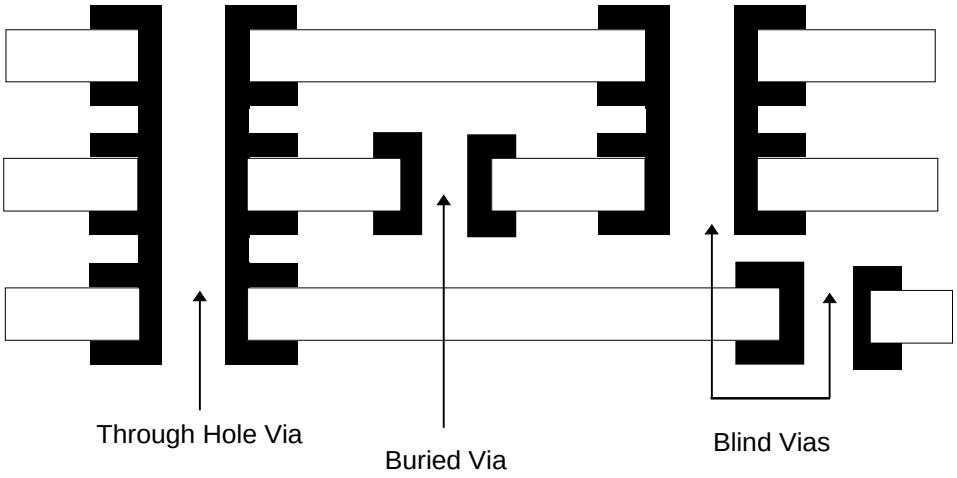
Section F: **BLIND AND BURIED VIA (BBV) BOARDS**

General description

Like through holes in a conventional multilayer board, blind and/or buried vias are holes that make connections between layers. However, unlike in a conventional multilayer board, blind and buried vias allow circuits of non-planar topography to be connected. This is important, as it conserves circuit board real-estate because it allows only necessary layers to be connected.

REYcomp uses the following terminology to define different types of drilled interconnection:

- A **through hole via** has access to both external layers.
- A **blind via** does not pass through the entire board, and has access to only one external layer.
- A **buried via** provides connection within inner layers, it has no access to the external layers.



Example of 6 Layer BBV Board

BBV Design Constraints

- U.L. limitation of a maximum of three thermal press cycles. The above example requires two such cycles: First, to laminate layers 1/2 to 3/4; second, to laminate layers 1/2 and 3/4 to 5/6.
- Core thickness 0.003 minimum.

Note: 0.5 ounce copper is required for BBV layers. Individual BBV layers will receive 0.0007 inch electrolytic copper during the through-hole plating process, bringing the total copper thickness to 0.0014 inch.

- Minimum drill size 0.0079 with a maximum aspect ratio of 7:1 for blind/buried via substrates.

  Note: All BBV holes will be plugged with epoxy during subsequent lamination cycles.

- The ability to register drilled holes to inner layers is impacted after each lamination cycle.

Minimum Annular Ring:	Drilled before first press cycle	- 0.004 inch per side
	Drilled after first press cycle	- 0.004 inch per side
	Drilled after second press cycle	- 0.006 inch per side
	Drilled after third press cycle	- 0.009 inch per side

- Multilayer design recommendations as outlined on page B11 apply.

Required information on drawings:

- The hole chart must list plated through holes separately from the BBV holes.

Contact REYcomp for additional information concerning the design of BBV boards.

Section G: CONTROLLED IMPEDANCE

Characteristic Impedance

The characteristic impedance of a transmission line is dependent on the relationship of the conductor width, conductor thickness, dielectric thickness between conductor and ground-power reference planes, and the dielectric constant of the dielectric medium.

It is recommended that the designer contact REYcomp to discuss impedance needs during the initial design phase. This will enable mutual understanding of requirements and impact of material characteristics, such as specific Dk's and manufacturing processes, on needed impedance targets and tolerances.

The actual impedance may have to be tested via a small prototype build. This is often necessary when tight impedance tolerances are required, or in the case of small line widths and dielectric thicknesses, which are more sensitive to variations. A tolerance swing due to etching variations will be more significant for a 0.005 inch line width than for a 0.010 inch line, for example.

Line width and dielectric thicknesses should be documented as reference dimensions only. This will allow REYcomp to make small adjustments to both parameters in order to match impedance targets.

Note: If a line width modification is necessary, it will only be accomplished globally. That is, all of the lines of the same width will be modified on a given layer. No modification will be made without prior consent of the customer.

For impedance calculations, it is important to consider the Etch Factor, the effective reduction of the line width during the etching process. (See Page C8). The exception to this is with boards with an Aspect Ratio GE 4.5:1 or with boards GE .090 inch thick and an Aspect Ratio of GE 3:1. No Etch Factor needs to be considered in these cases.

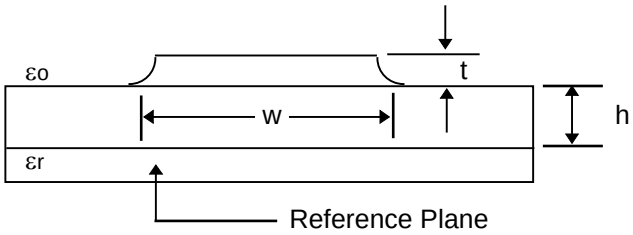
The recommended impedance tolerance is +/- 10 %. A lesser tolerance is often achievable, especially with fully embedded Microstrip and Stripline structures. This requirement must be discussed with REYcomp for appropriate focus.

Changes in physical parameters will affect impedance as follows:

As Physical Values Change		Impedance Will Move
Dielectric Constant	↓	↑
Dielectric Thickness	↑	↑
Line Width	↓	↑
Line Thickness	↓	↑

Impedance Structures

Surface Microstrip



The microstrip line is a popular transmission line structure for high speed digital circuits. The Surface Microstrip location on the external layer is subject to potentially greater impedance variables. This is due to the additional copper electro-plating it receives, resulting in increased line thickness and line width tolerances.

For microstrip lines that are very wide ($w \approx >1.0$ inch) the ε_{eff} will become almost equal to ε_r. For very narrow lines ($w \leq 0.005$ inch) the ε_{eff} will be approximately the average of ε_r for the dielectric material and air, i.e. $\varepsilon_{eff} \approx 0.5\ (\varepsilon_r + 1)$.

For Microstrip applications, the following formula will provide approximation of impedance:

$$Zo = \frac{87}{\sqrt{\varepsilon_{eff} + 1.41}} \ln \frac{5.98h}{0.8w + t}\ \Omega$$

where: Zo Characteristic Impedance; ε_{eff} Effective Dielectric Constant; h Dielectric Thickness;

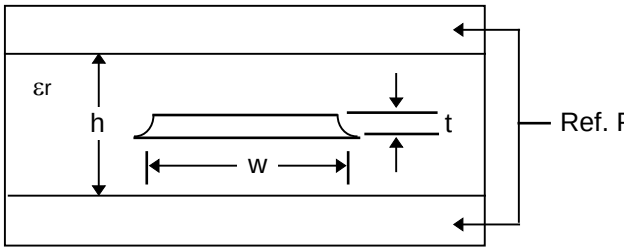
w Line Width (avg.); t Line Thickness (including plated copper)

For critical applications, the Microstrip line can be embedded in dielectric material. The impedance can be calculated from the Surface Microstrip formula. Then for each .001 inch below the surface, subtract 1% of the impedance calculated. This derating factor provides good results for embedding up to approximately .015 inch. A thicker embedding has little additional effect.

Impedance Structures, continued

Stripline

The stripline is embedded in dielectric material and is sandwiched between two reference planes. This configuration significantly reduces cross talk effect. This structure is most suitable for improving impedance tolerances.



For Stripline applications, the following formula will provide close approximation of impedance:

$$Zo = \frac{60}{\sqrt{\varepsilon r}} \ln \frac{4(2h + t)}{2.1(0.8w + t)} \ \Omega$$

where: Z0 Characteristic Impedance; er Dielectric Constant of material; h dielectric thickness; w Line Width (avg.); t Line Thickness

Another commonly specified structure is the **Dual Stripline**. No formula has been found that accurately accommodates a wide range of structure thicknesses. For this type of transmission line REYcomp has developed empirical data for correction. For impedance modeling of this type and other complex single ended or **Differential** transmission lines, please contact REYcomp.

Impedance Test Pattern

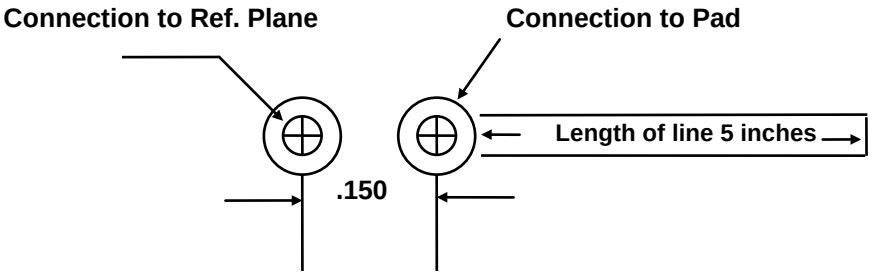
Actual Impedance will be measured via the TDR (Time Domain Reflectometry) method.

Suitable test lines need to be provided by the designer for each layer with impedance requirements. These lines need to be a minimum of 3.0 inches long (ideally 5.0 inches) without networking into another layer. They also need to be accessible from the external layer with a .030 minimum diameter hole, and be within .150 inch of another hole of the same diameter, making connection to the reference plane.

Formulas per ANSI/IPC-D-275 Design Standard for Rigid Printed Boards (September 1991)

Impedance Structures, continued

In the absence of a customer supplied test line, REYcomp will add a suitable test coupon to the panel. With appropriate panel location and line widths, it will be closely representative of the actual board. This coupon will serve as the referee for the acceptance of impedance requirements. Coupon may be identified, in order to retain its relationship to the panel, if required.



Impedance Test Pattern

Note: For the test pattern, REYcomp will select appropriate hole size from the circuit board drawing.

Section H: TESTING

Testing

Three main test parameters are of interest to customers:

Test Voltage

The amount of power applied to the circuit for testing.

Continuity Resistance

The maximum resistance allowable for a circuit. Any higher resistance indicates a possible open circuit.

Isolation Resistance

The minimum resistance allowable between separate electrical entities. Any lower resistance indicates a possible short.

Testable settings for these parameters are system dependent. The following table identifies the three systems currently available for new designs, the ranges for the parameters on each system, and the maximum testable size for each system.

System Max.	Test Voltage	Continuity Resistance	Isolation Resistance	Testable Size	
TRACE 948	100v	10 - 600 ohms	1.67 - 100 Megohms	23”	17”
TRACE 948 Large Bed	100v	10 - 600 ohms + TSR	600 - 2.5 Megohms	22”	16”
TRACE 948 Small Bed	10v	10 - 600 ohms + TSR	600 - 2.5 Megohms	11.9"	17"
ATG TR-1000	10-200v	10 - 100 ohms + TSR		18"	12"
TG-4400	10-250v	5 - 1 ohms	100k - 100 Megohms	18"	24”
ATG A-1000	10-250v	10-100 ohms	100k - 10 Megohms	16”	20”

Note: TSR, Test System Resistance, ranges from 2.5 to 6.5 ohms. TSR must be added to stated continuity resistance values to obtain true testable ranges. For example, on TRACE 948, when TSR is 5.03 ohms, true continuity resistance testable range is 8.03 - 605.03 ohms.

Note: It is possible for a test to indicate both open and short between the same test points. When this happens, the board is treated as possibly defective and verified manually.

A Flying test probe is available for orders with less than 72, 000 test points total. This is the equivalent of 12 boards with 6000 test points each. One-time builds or once a year builds would be candidates for this fixture-less test. This test is subject to scheduling availability, since each test takes so long.

VOLTAGE	RESISTANCE RANGE	TESTABLE SIZE
10 - 500v	50 ohms to 100 Megohms	24" & 27"

DESIGN REQUIREMENTS FOR CONTINUITY TESTING OF FINE PITCH DEVICES:

To facilitate effective testing of fine pitch SMD devices, down to 0.020 inch ctc. pitch, a few critical rules must be followed during the design of the board.

Minimum Pitch - The minimum center-to-center distance for SMD pads is currently set at 0.020 inch.

Minimum Pad Length - (Refer to figure 1.) The minimum pad length for all SMD pads is currently set at 0.070 inch.

Grid Location Availability - (Refer to figure 2.) The number of test points, through-holes or SMD pads, in a given area of the board, are limited to the number of test machine grid locations in the same given area. That is, for every test point on a board, there must be a unique test grid location within 0.200 inch. When a unique grid location is not available, the test point cannot be tested. This is normally not a problem except when too many SMD pads are located within a very small area.

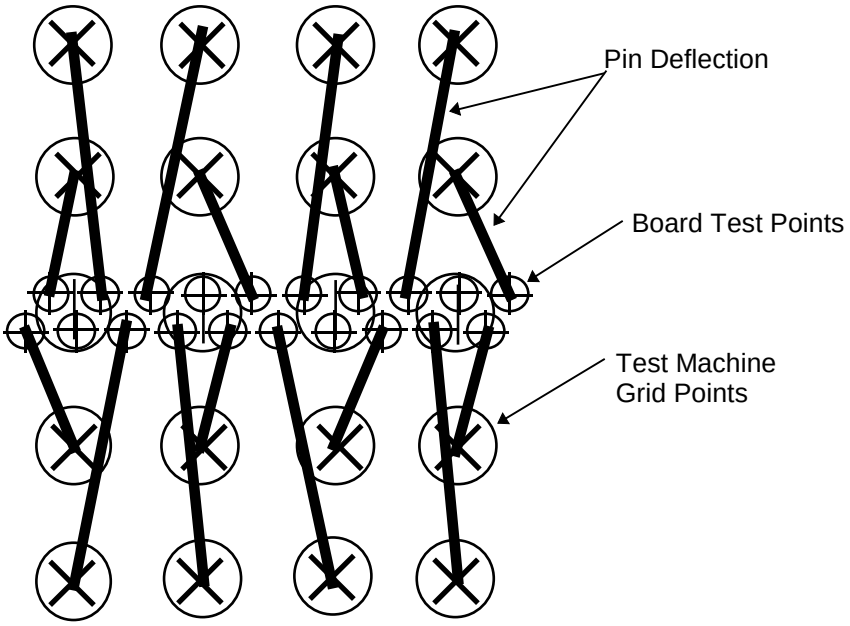


Figure 1

Figure 1 illustrates this problem by showing one side of a typical 0.020 inch pitch device overlying a 0.100 inch grid of test machine grid locations. For every 0.100 inch down each side of the device, there are five SMD pads, test points. To test all the pads, a swath of five test machine grid locations must be reserved for each side of a 0.020 inch pitch quad-pack. Then, pads for two 0.020 inch pitch devices can be located no closer than 0.500 inch, with absolutely no other test points, e.g. resistor or capacitor pads, in between. If the quad-packs are closer than 0.500 inch, or if other test points are placed in between, then some test points cannot be tested. Similarly, a swath four locations wide is required for each side of a 0.025 inch pitch device. Then, two 0.025 inch devices can be located no closer than 0.400 inch, with no test points in between.

For 100% testing, there cannot be more test points in a particular area of a board than there are machine grid points in a particular area of a board.

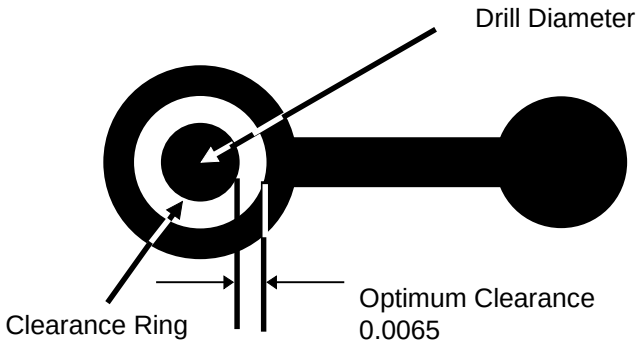
Board-to-Fixture Registration - To facilitate good board-to-fixture registration there should be three unplated holes of sufficient size, 0.070 inch to 0.155 inch diameter, positioned such that lines connecting the holes form a triangle. The footprints for all fine pitch devices should fall within or on that triangle. The reasoning behind this is that board movement will be less near the centroid of the triangle.

To help with timely netlist generation, avoid large drawn areas in the gerber data, especially on plane layers. Flashed SMD pads on outerlayers need to be utilized.

Beep Test Coupon

The use of a beep test coupon for the purpose of electronically testing inner layer registration is occasionally employed. The following design rules must be adhered to:

- The clearance diameter must be sized in a manner that takes into consideration etching capability based on copper weight (ounce). The clearance diameter should be determined at the foot of the etched feature. The clearance must be a minimum of 0.001 inch larger than the minimum annular ring diameter. This prevents beep test failure at tangency and provides allowance for etch tolerance. The optimum beep test clearance diameter should be no less than 0.013 inch larger than the drill diameter used to drill the hole within the feature.
- Optimum drill diameter used to drill the clearance feature of the coupon should be between 0.030 and 0.070 inch.
- Specify only one beep test coupon per corner of panel (4 total).



Beep Test Pattern

Section I: UNDERWRITERS LABORATORIES INC. (UL) APPROVAL MARKING

Recognition and Flammability Ratings

UL recognition means that boards of specified base materials and design, and manufactured through identified processes, have been investigated by Underwriters Laboratories Inc. for thermal shock, bond strength and plating adhesion. Details of this investigation are in the UL 796, Standard for Printed Wiring Boards.

Flammability Classification

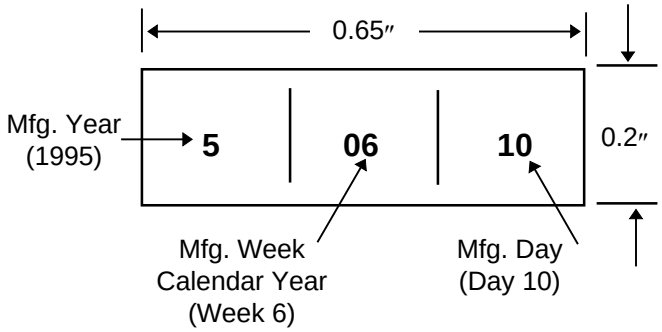
Flammability classification means that boards of specified base materials and design, manufactured through identified processes, have been investigated and classified by Underwriters Laboratories Inc., for flammability according to UL 94, Standard for Tests for Flammability for Parts in Devices and Appliances.

Design Guidelines

Each design should provide space on the outer layer for a UL recognized marking as described in the UL recognized Component Directory, UL Yellow Card, or UL report. It is the responsibility of REYcomp to mark the boards appropriately. The customer must indicate the UL requirement either in their specifications and standards or on the drawing.

Lot Code Marking

Many customers require that REYcomp provide a lot code. Our lot code is deciphered as follows:



Section J: GUIDELINES FOR TOOLING INTERFACE

The successful transformation of printed circuit board design data into manufacturing tools depends on the quality of the data received and the quality of decisions made in its interpretation. This process is complicated by a wide variety of data communication styles and format.

We strongly recommend that system compatibility and data-set completeness be reviewed and tested before production tooling. Sending a complete “non-production” part design through the tooling process reduces the possibility that production will be delayed when time is critical.

Along with a description of the minimum requirements, more specific guidance is offered regarding data options and preferences in the form of tooling capability classes. Below is a brief explanation of the meaning of each of these classes.

TOOLING CAPABILITY CLASSIFICATION

PREFERRED

Part data whose characteristics facilitate smoother, high quality tooling design processing. The part data sets that fall into this category minimize the risk of miscommunication because they require less human interpretation, allow greater process automation, have reduced data volumes, and use simpler communication protocols.

ACCEPTABLE

Part data whose characteristics are less than optimum, but are within our normal tooling design capability.

STRONGLY DISCOURAGED

Part data whose characteristics push the limits or fall outside the range of our normal tooling design capability. Because of the increased demand on our resources and the increased risk of communication failure, the tooling of these parts must be negotiated with your REYcomp Account Manager.

REYcomp is a strong advocate of the IPC-D-350 data format for exchanging circuit board design information. This standard format contains all image and NC data in a single integrated file. The highly defined structure of this data format streamlines design-to-manufacturing communication by eliminating the need for the coordination of multiple files and interpretation of vendor-specific data formats. For more information about the advantages offered by IPC-D-350 please contact your REYcomp Account Manager.

IMAGE DATA

The image data is a graphic description of the part used to create the photo-tools. The **minimum requirements** for tooling image data are:

1. At least one image film supplied for each piece of artwork.
2. A clear description of the function of each file.
3. Image file merging, if required, must be clearly described.
4. If Gerber format is used, a table clearly describing the aperture shapes and dimensions, along with their assorted Gerber D-code must be supplied.
5. Custom, non-standard apertures must be clearly and completely described. A large number of customer apertures may require a tooling surcharge.
6. If Gerber format is used, the format information must be supplied. This should include a description of coordinate format, coordinate mode (absolute or incremental), and zero suppression.

PREFERRED

- Gerber or IPC350 format
- File function described both within the image data and in explanatory documentation.
- Pads “flashed” with standard aperture shapes rather than “painted” with lines.
- Soldermask pads the same size as the outer layer pads allowing easy modification to manufacturing specifications.
- Direct transfer of the original CAD system aperture table file, allowing automated translation of aperture data.
- ASCII data code.

ACCEPTABLE

- “Painted” pads.
- Image files not in alignment.
- “Standard aperture” table to be used for all parts. Part specific deviations communicated via the job order.
- Aperture table with each order that is not machine readable.
- File function described with naming convention or explanatory documentation.
- EBCDIC data code

STRONGLY DISCOURAGED

- Image data supplied with filmwork only.
- Missing or ambiguous data.
- Multiple aperture tables.
- Custom editing of conductive features.
- Very large files, usually caused by inefficient “painting” of image fill areas.
- Format other than Gerber or IPC350.

PROFILE DATA

The rout profile program is created by interpreting the part’s fabrication drawing. This drawing must clearly and fully describe the part profile using standard dimensioning and tolerancing practices. It must also provide a dimensional reference to at least one drilled hole internal to the part.

PREFERRED

- Drawing files supplied in HPGL format with compatibility fully tested before use.

ACCEPTABLE

- Drawing files supplied in Gerber, IGES or DXF (v.11 or earlier) format, fully tested before use.
- Paper fabrication drawing.

STRONGLY DISCOURAGED

- Plotter compatibility not fully tested before use.
- Incomplete dimensioning of the part.

DRILL DATA

REYcomp uses the drill program provided as a master from which the production drill program is produced. The **minimum requirements** for tooling drill data are:

1. At least one file describing the location of all holes internal to the part.
2. A drill shop report must be provided that includes the following information for each hole size:
    - Finished hole size.
    - Finished hole-size tolerance.
    - Hole count.
    - Hole plating status.

A drawing of drilled hole locations should be provided which represents each drilled hole size with a unique symbol or letter to verify the correctness of the drill data.

PREFERRED

- Drill data provided in Excellon format 2 or IPC350 format.
- The order of holes drill shop report matches the order in the drill data.
- Drill data aligns with image data.
- ASCII data code.

ACCEPTABLE

- Drill data supplied in Gerber format.
- EBCDIC or EIA code.

STRONGLY DISCOURAGED

- Paper tape
- A plot for the drilled holes is not provided.

MEDIA OPTIONS

PREFERRED

Part data supplied using one of the following media:

- Modem (300/1200/2400/9600/19200 baud)
- 3 1/2 inch disk (MS-DOS)
- 5 1/4 inch floppy disk (MS-DOS)
- 150 MB 1/4 inch streamer tape (UNIX)
- 2/5 GB 8mm tape (UNIX)

STRONGLY DISCOURAGED

Part data supplied using one of the following media:

- Paper tape
- Image data supplied with filmwork only.
- Other media

DATA COMPRESSION OPTIONS

If data compression is used, a description of the compression technique used should be included in the data set.

PREFERRED

Part data supplied in one of the following data compression formats:

- pkzip (MS-DOS, SUN)
- tar (UNIX)
- cpio (UNIX)
- compress (SUN)
- bar (SUN)

STRONGLY DISCOURAGED

Part data supplied using other data compression formats.